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(54) ORGANIC LIGHT EMITTING DISPLAY AND MANUFACTURING METHOD THEREOF

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**^{7} **H05B 33/00**

(52) **U.S. Cl.** **313/504**; 313/506

(57) **ABSTRACT**

An organic light emitting display is provided, which includes: a first electrode formed on a substrate; a partition having an opening exposing the first electrode at least in part; an auxiliary electrode formed on the partition and having substantially the same planar shape as the partition; an organic light emitting member formed on the first electrode and disposed substantially in the opening; and a second electrode formed on the light emitting member and the auxiliary electrode.

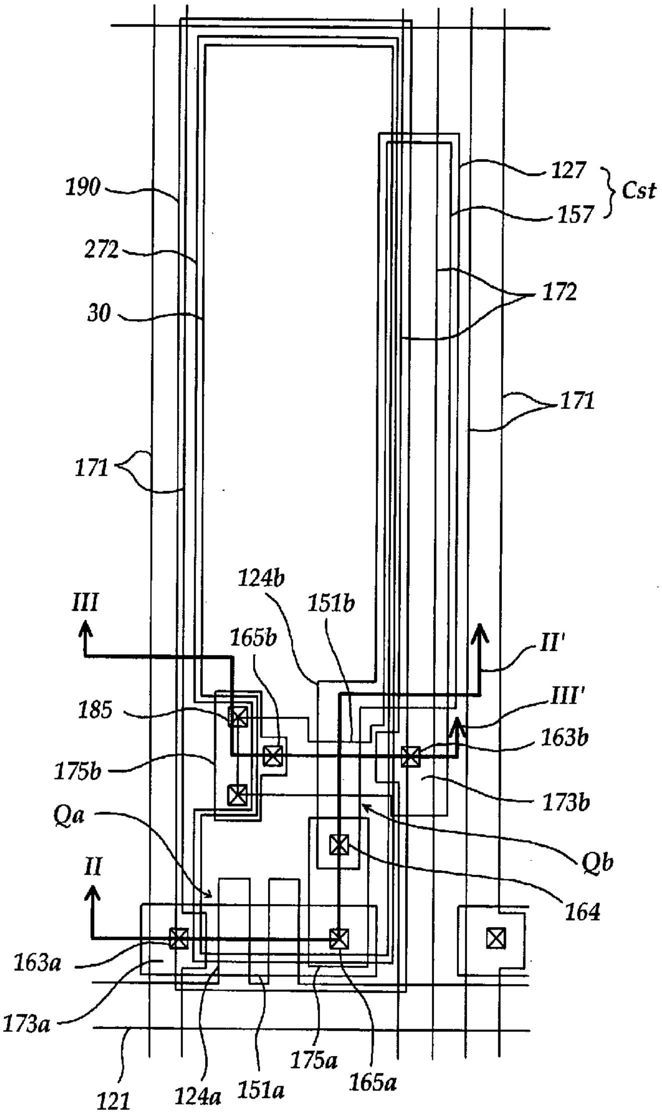


FIG. 1

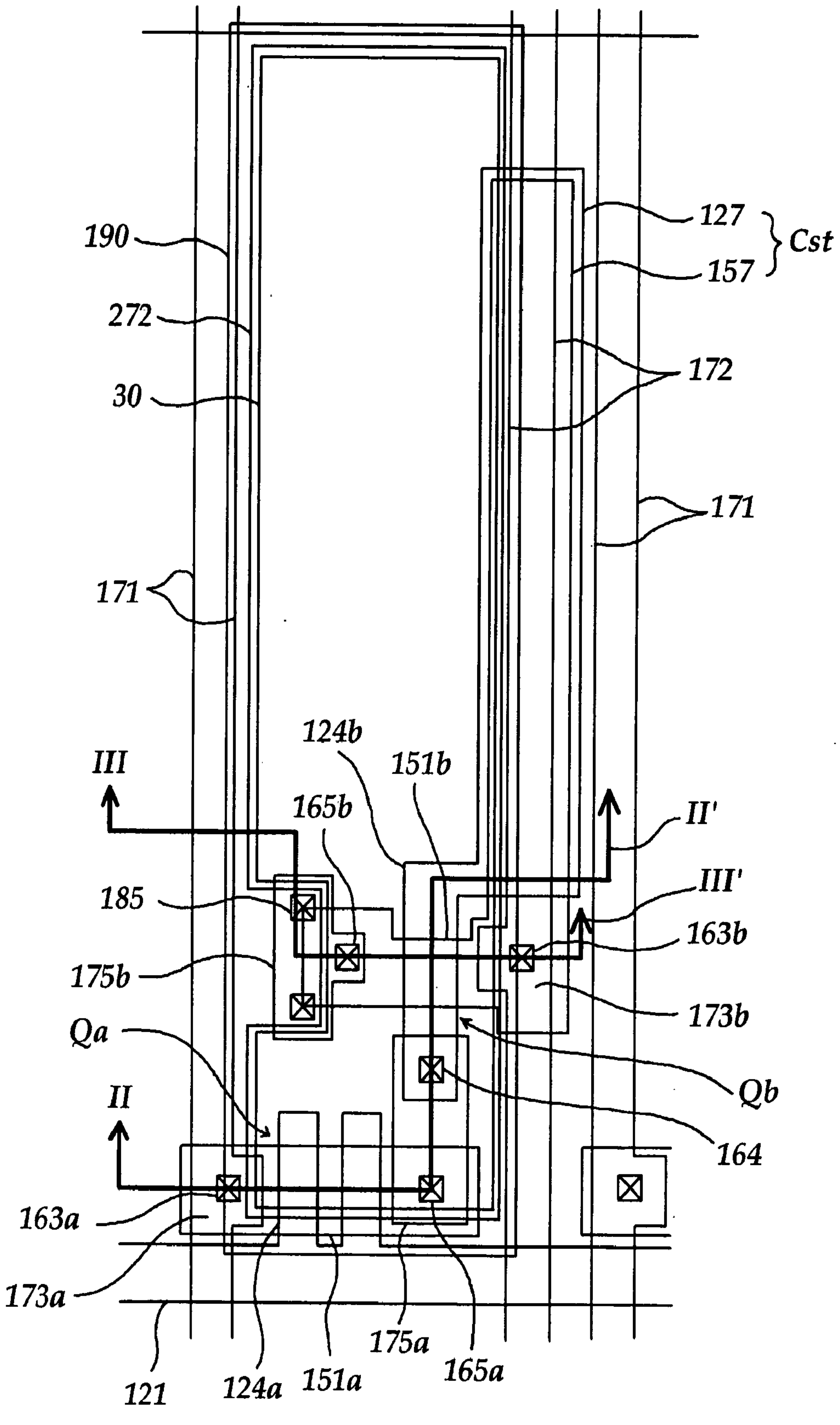

127
Cst
157
190
272
30
172
171
171
124b
151b
III
165b
II'
III'
185
163b
175b
173b
Qa
Qb
II
164
163a
173a
121
124a
151a
175a
165a

FIG. 2

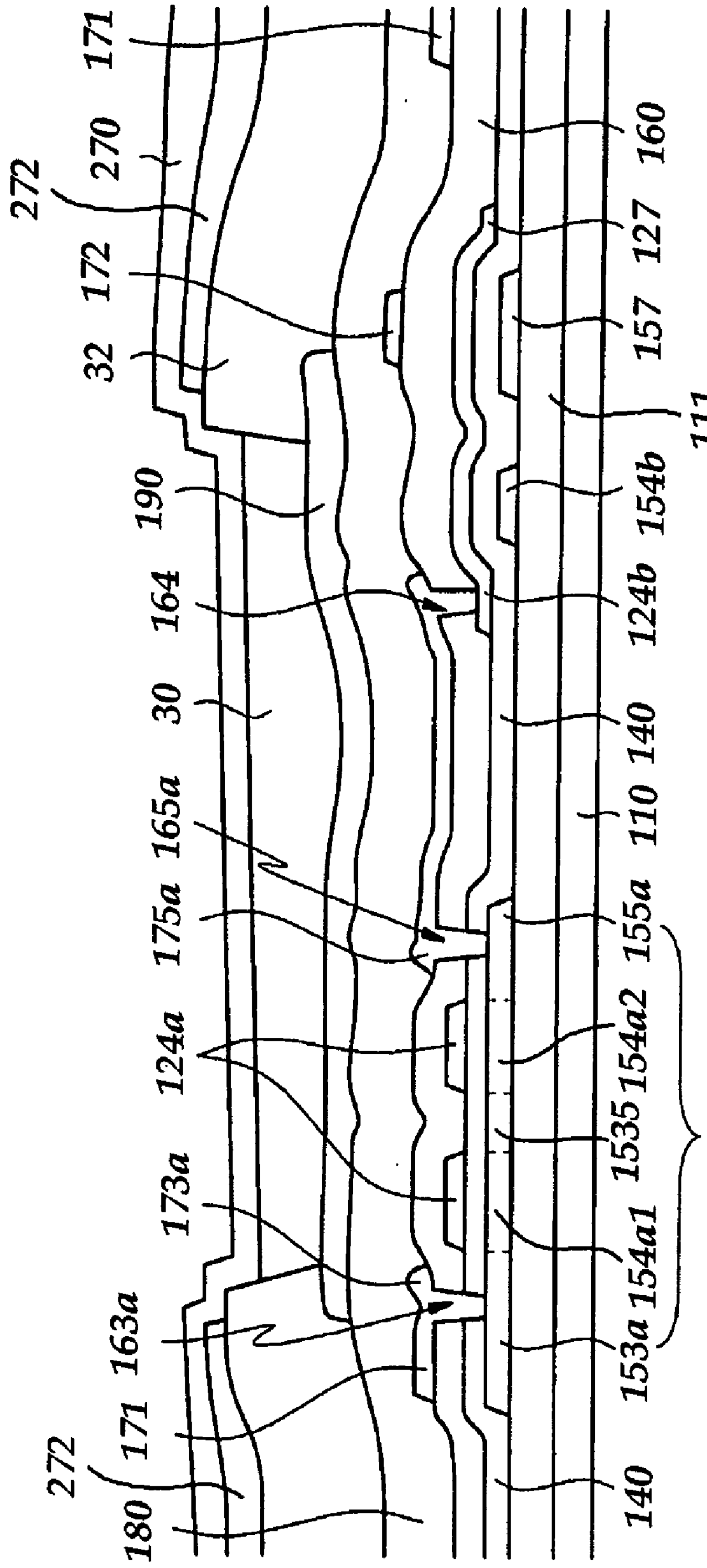

171
270
272
172
32
190
164
30
165a
175a
124a
173a
163a
171
272
180
160
127
157
111
154b
124b
140
110
155a
154a2
1535
154a1
153a
151a
140

FIG. 3

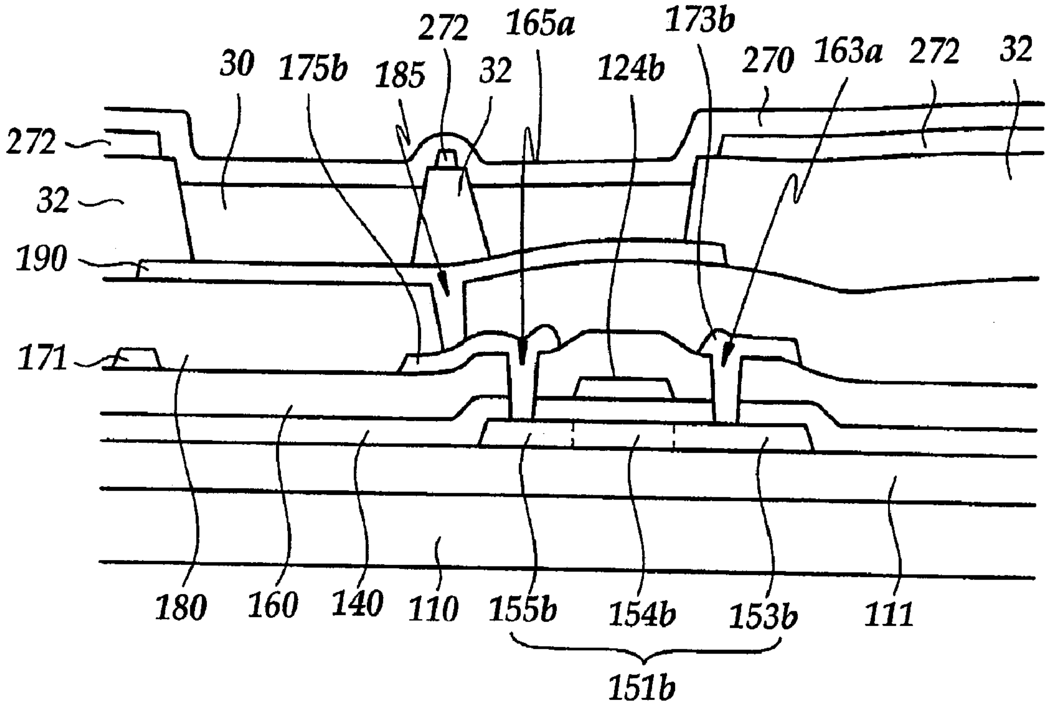

272
165a
173b
30
175b
185
32
124b
270
163a
272
32
272
32
190
171
180
160
140
110
155b
154b
153b
111
151b

FIG. 4

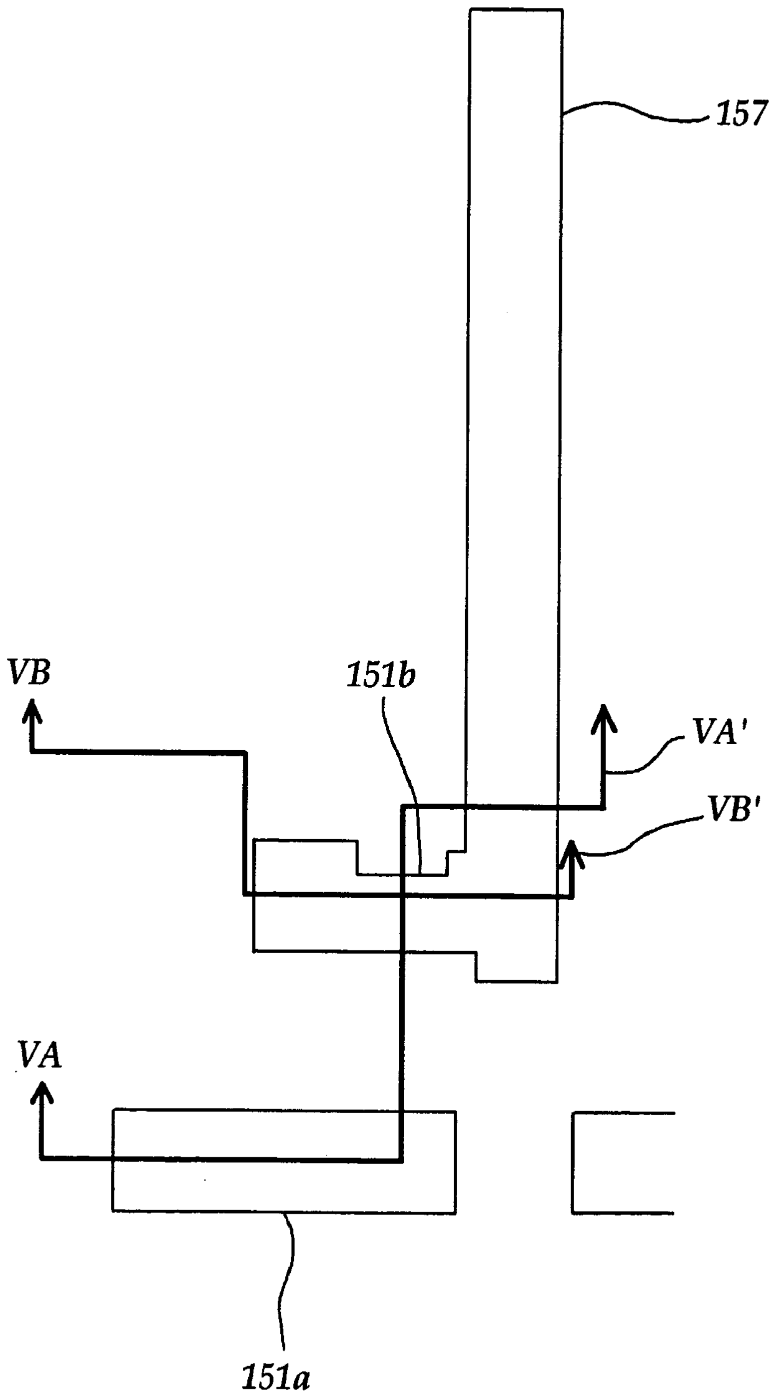


FIG. 5A

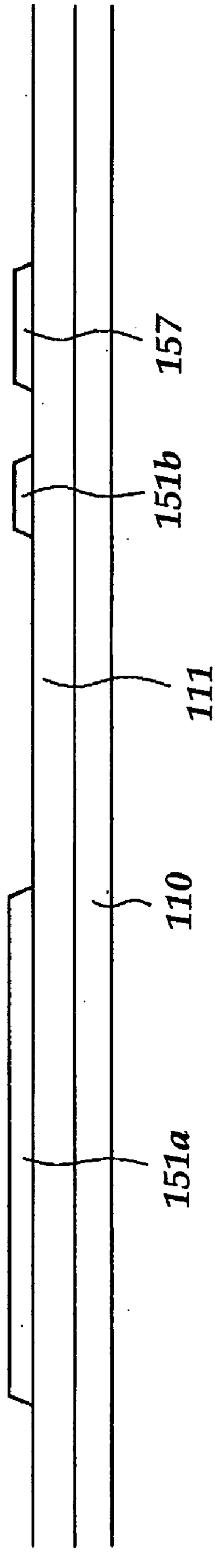


FIG. 5B

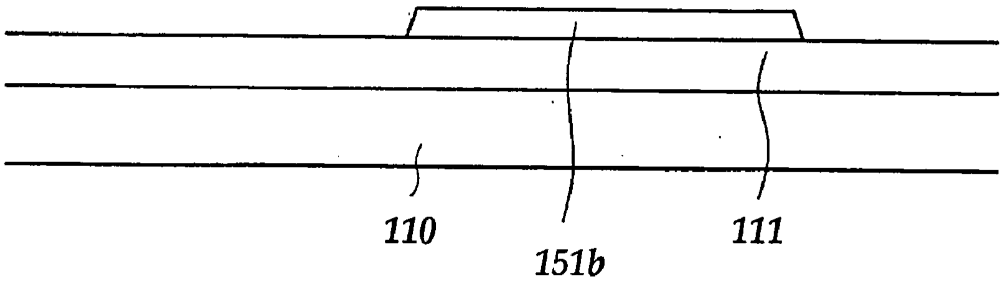


FIG. 6

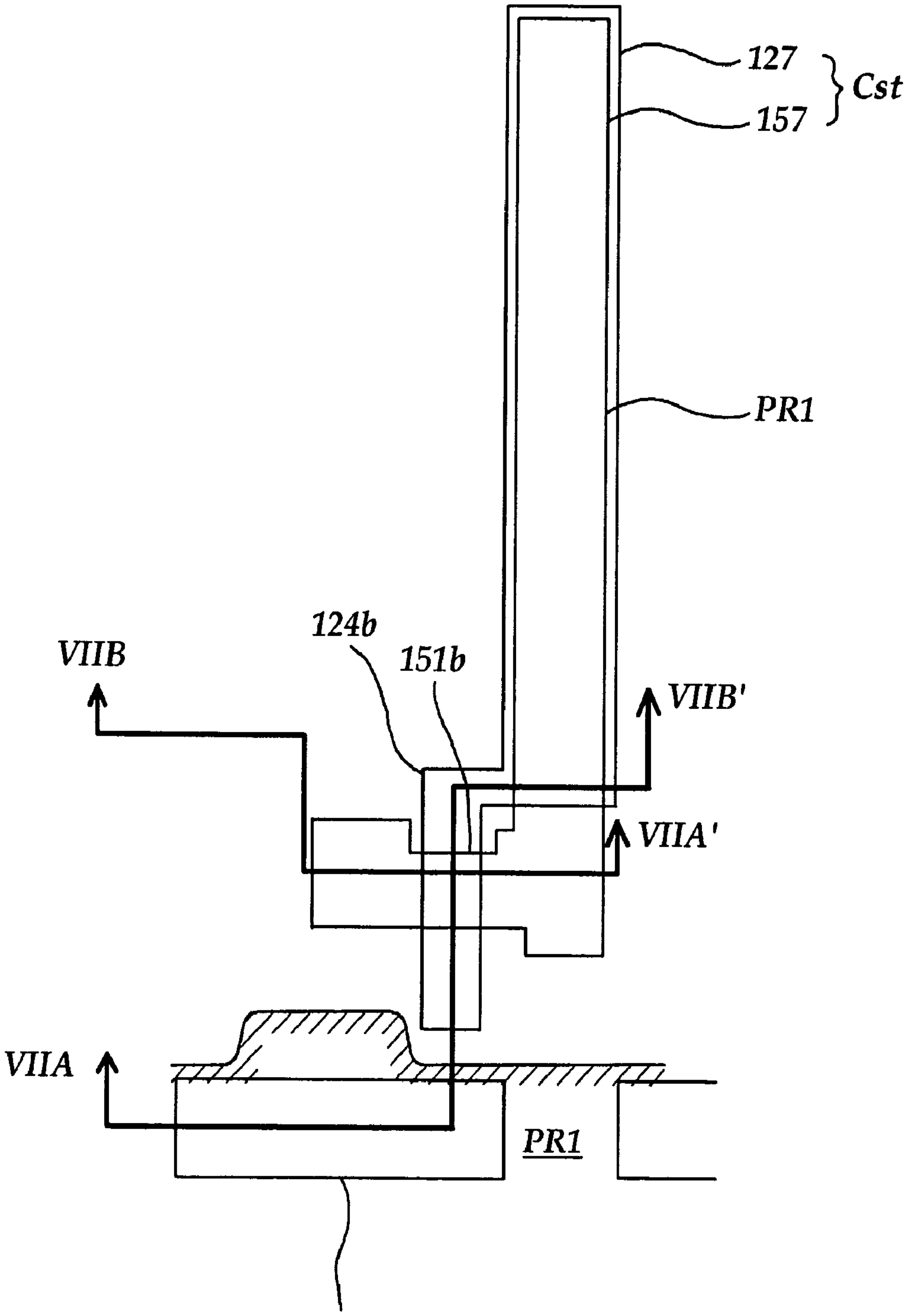


FIG. 7A

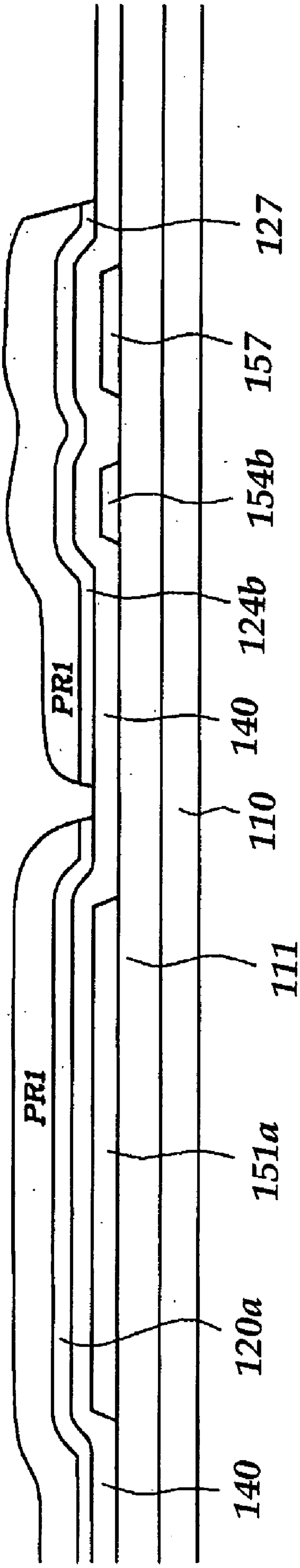


FIG. 7B

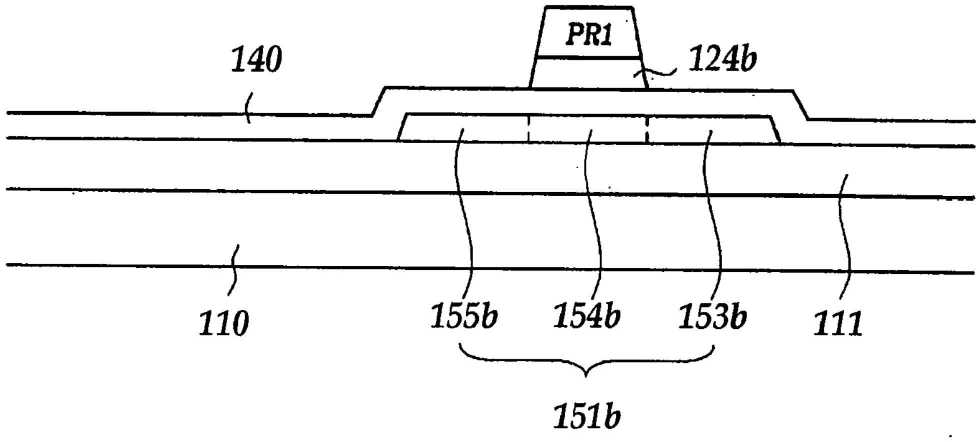


FIG. 8

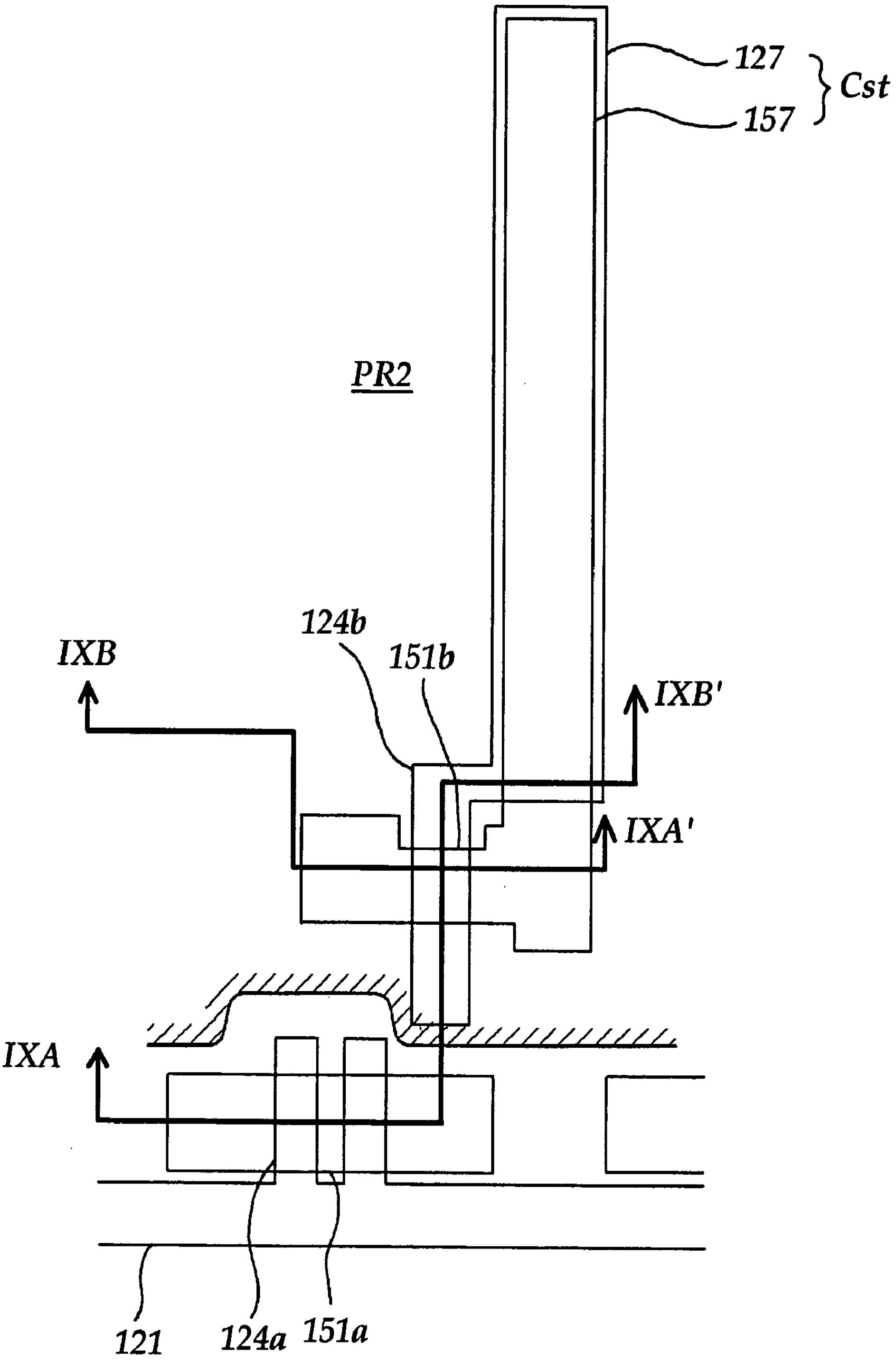


FIG. 9A

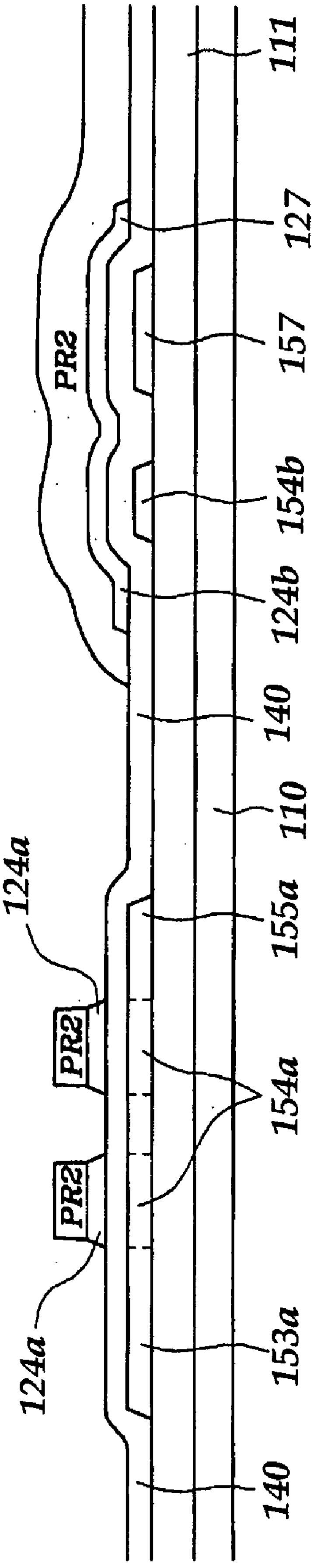

111
127
PR2
157
154b
124b
140
110
124a
155a
PR2
PR2
154a
124a
153a
140

FIG. 9B

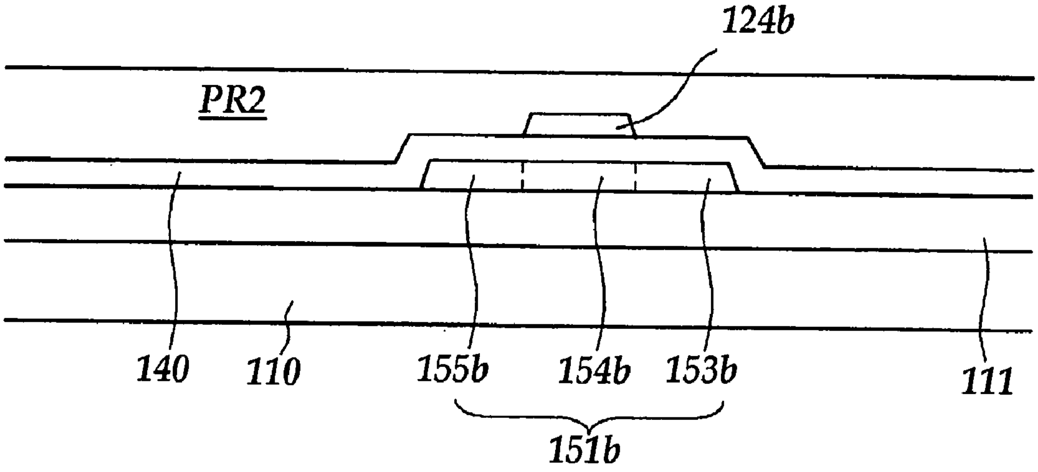


FIG. 10

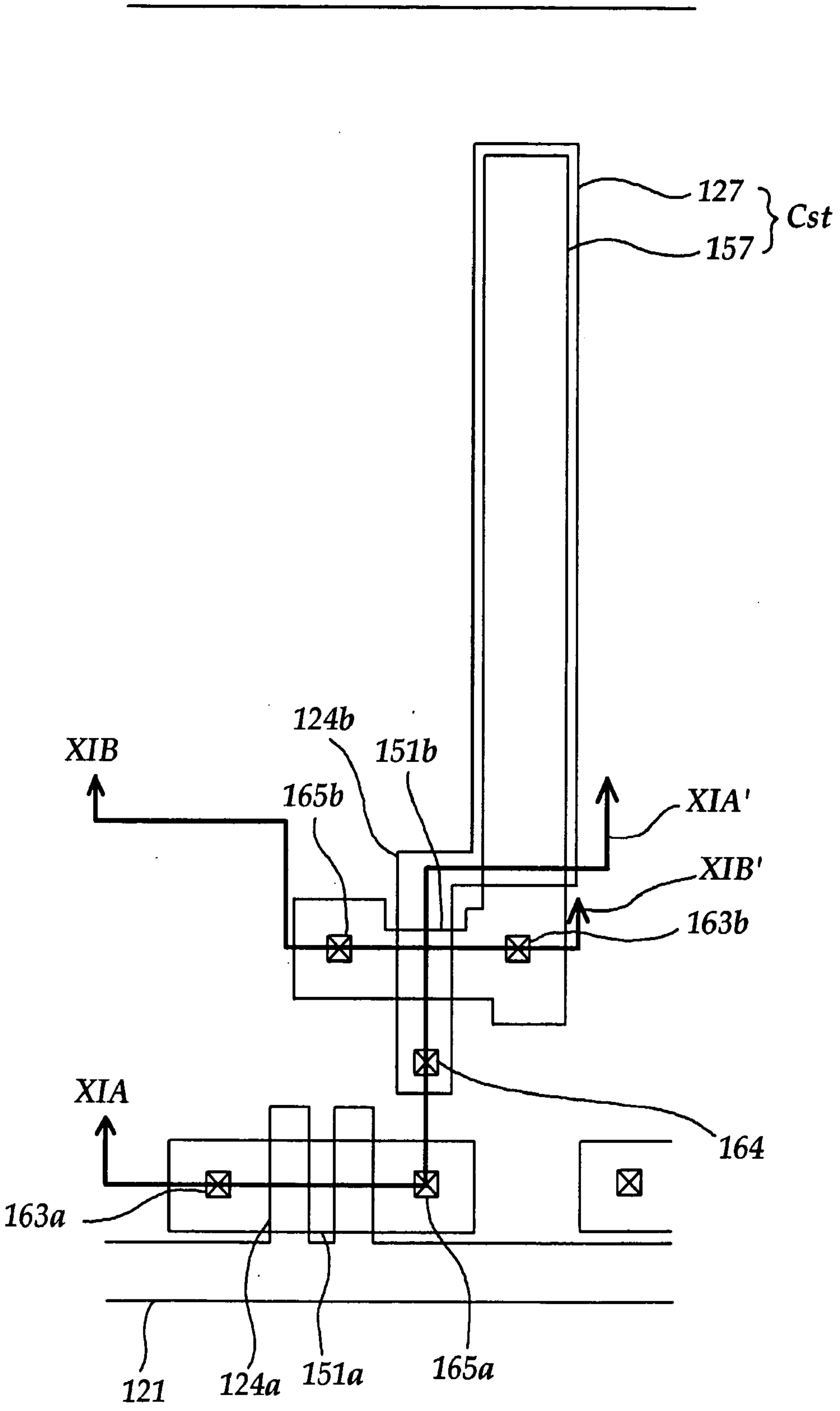

127
157
Cst
124b
XIB
151b
165b
XIA'
XIB'
163b
164
XIA
163a
121
124a
151a
165a

FIG. 11A

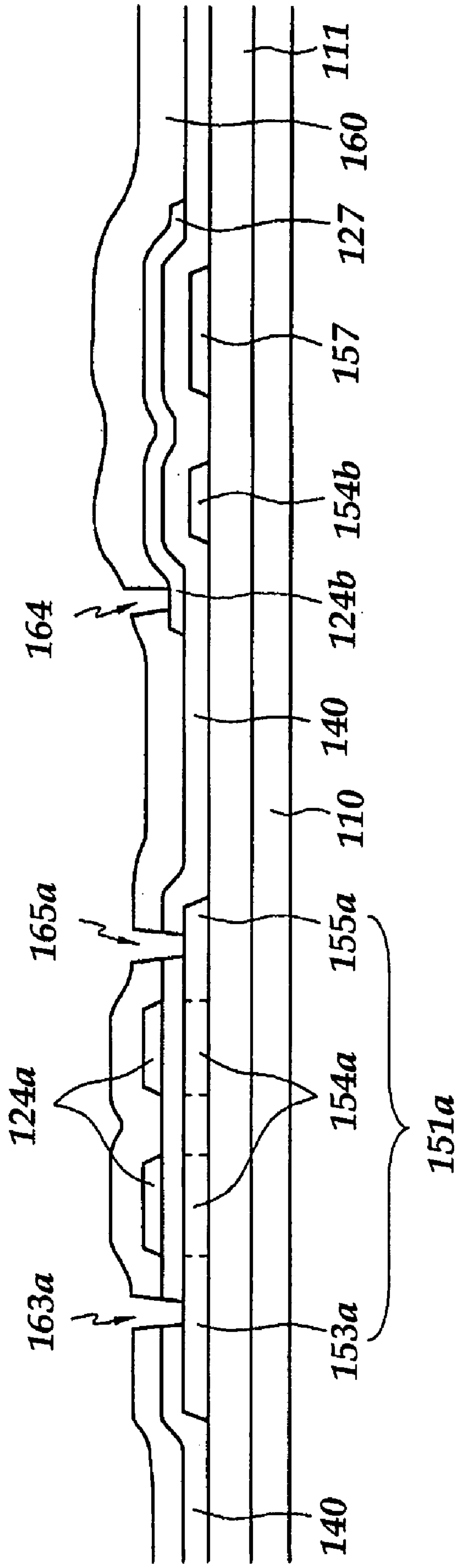

111
160
127
157
154b
124b
164
140
110
155a
165a
154a
124a
151a
163a
153a
140

FIG. 11B

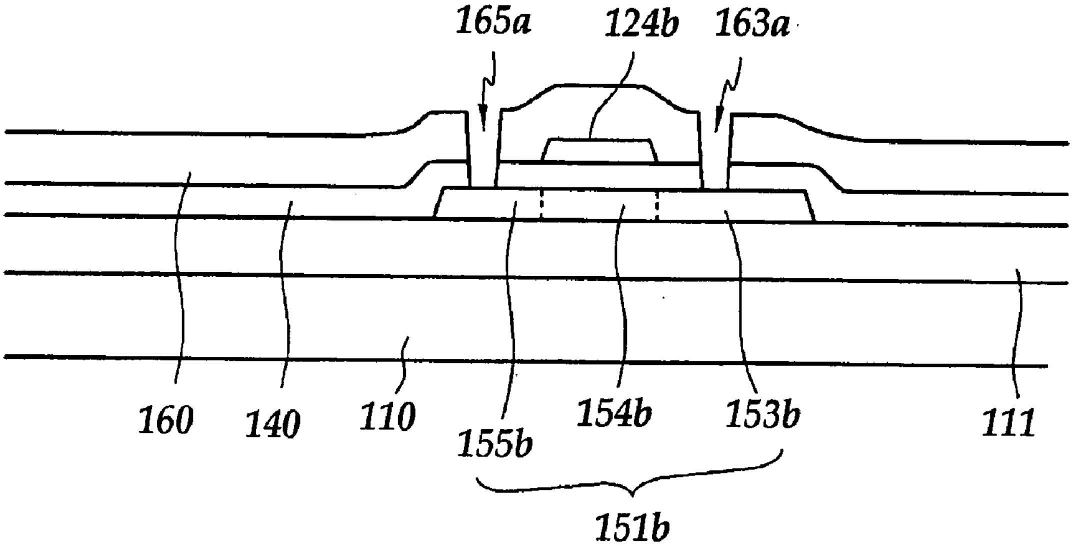


FIG. 12

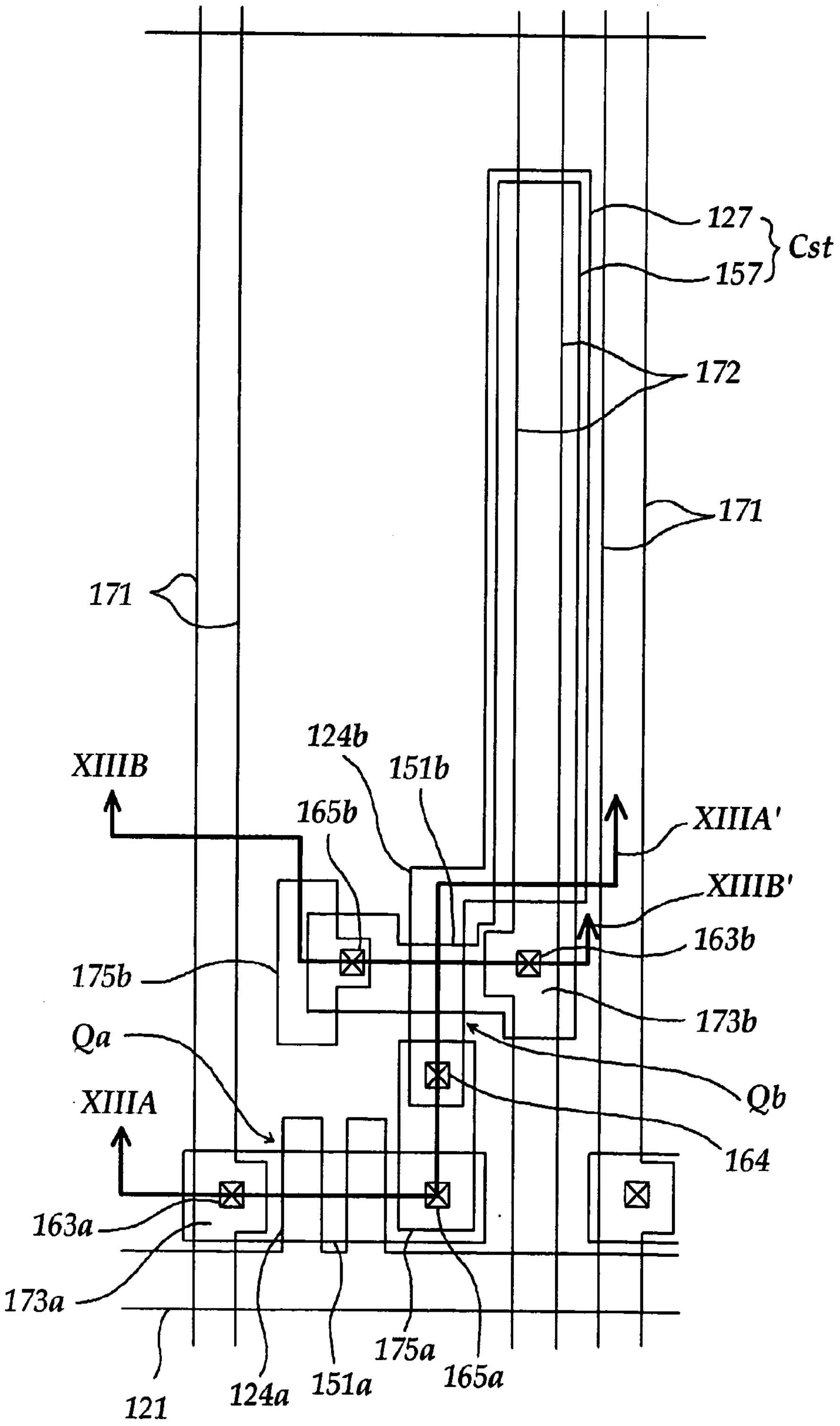

127
157
Cst
172
171
171
124b
151b
XIIIB
165b
XIIIA'
XIIIB'
163b
175b
173b
Qa
Qb
XIIIA
164
163a
173a
175a
121
124a
151a
165a

FIG. 13A

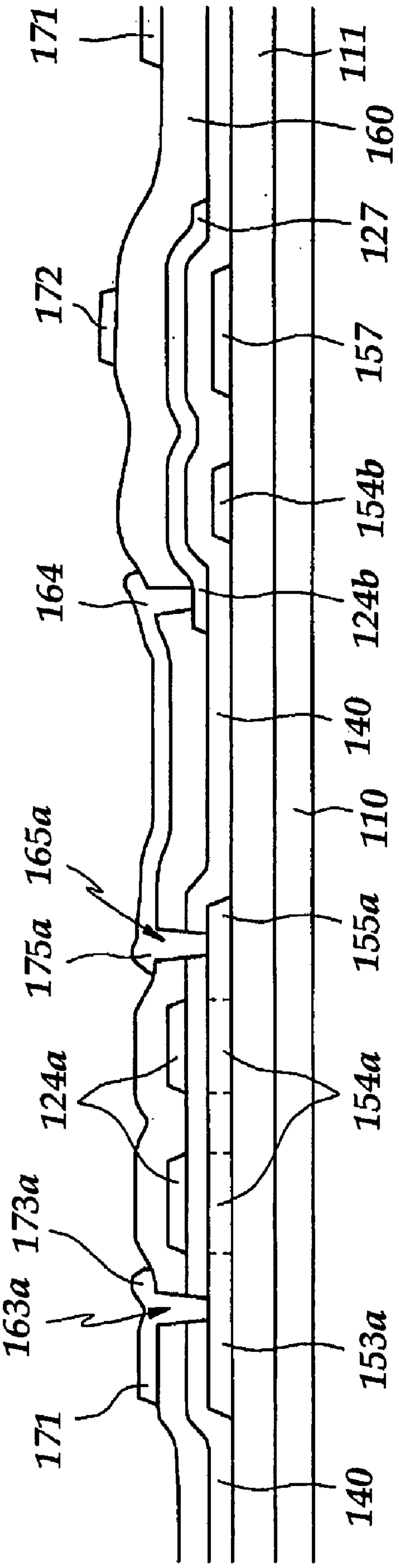

171
163a
173a
124a
175a
165a
164
172
171
140
153a
154a
155a
110
140
124b
154b
157
127
160
111

FIG. 13B

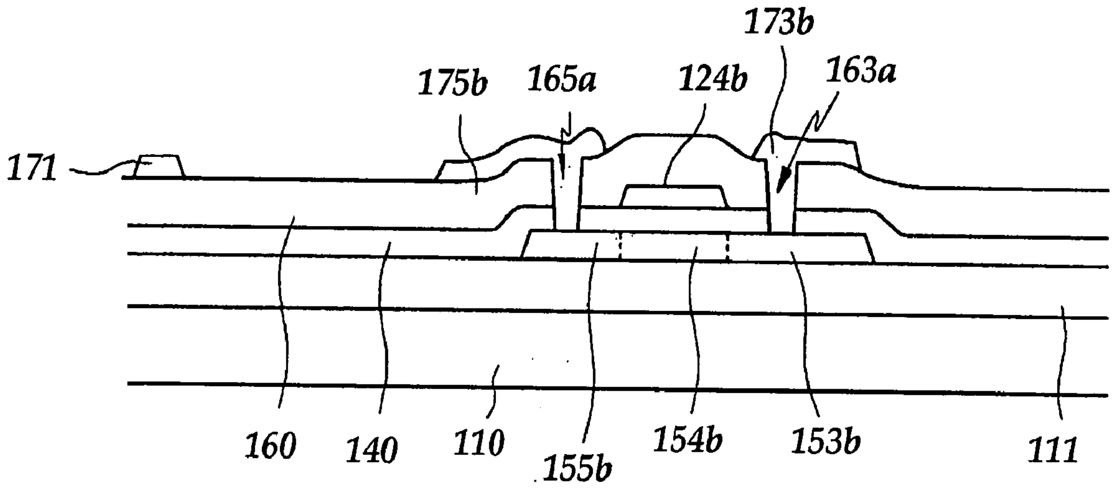


FIG. 14

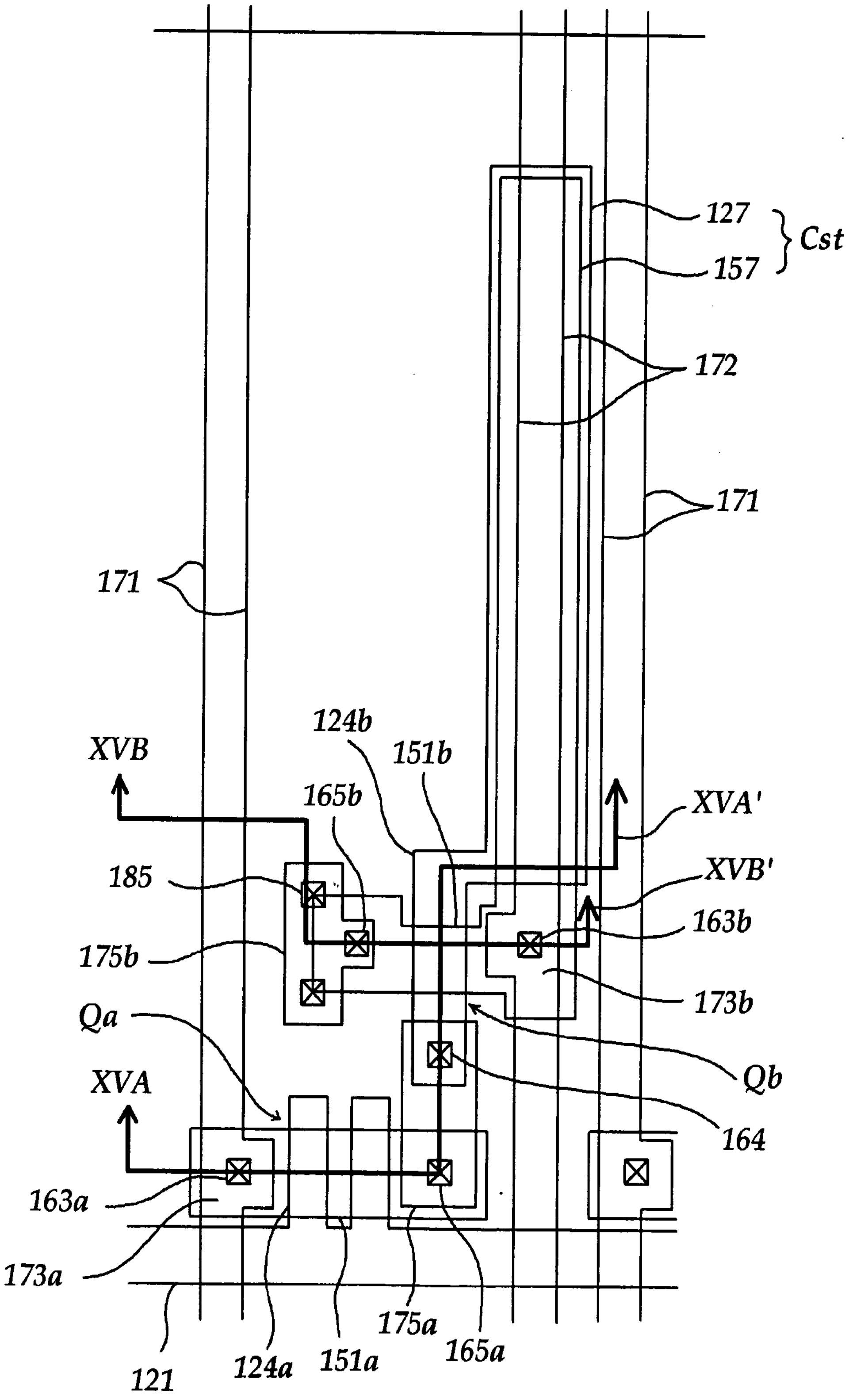

127
157
Cst
172
171
171
124b
151b
XVB
165b
XVA'
185
XVB'
163b
175b
173b
Qa
Qb
XVA
164
163a
173a
175a
165a
121
124a
151a

FIG. 15A

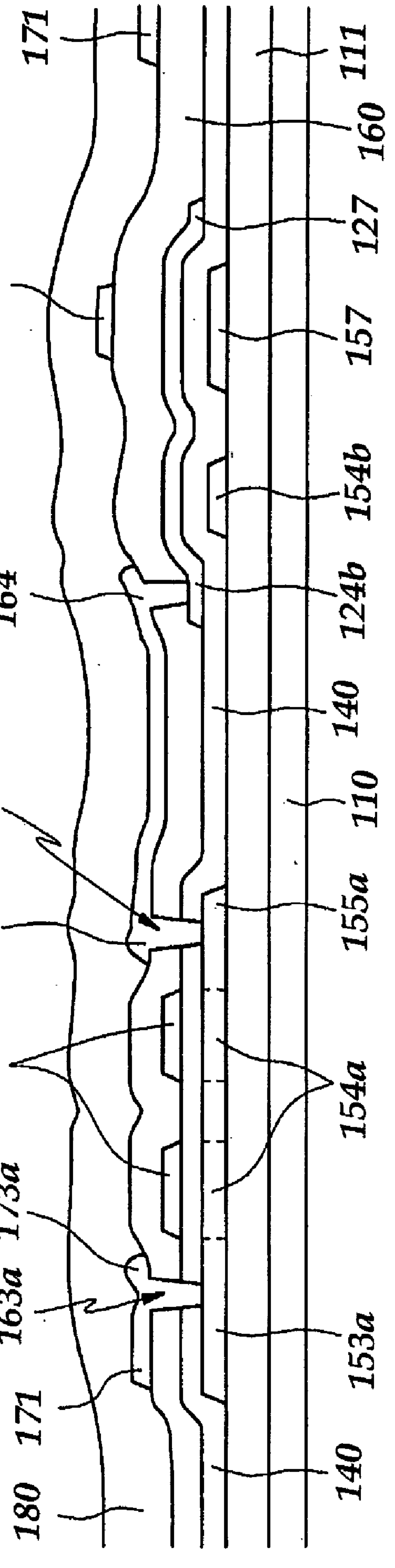

180
171
163a
173a
124a
175a
165a
164
172
171
140
153a
154a
155a
110
140
124b
154b
157
127
160
111

FIG. 15B

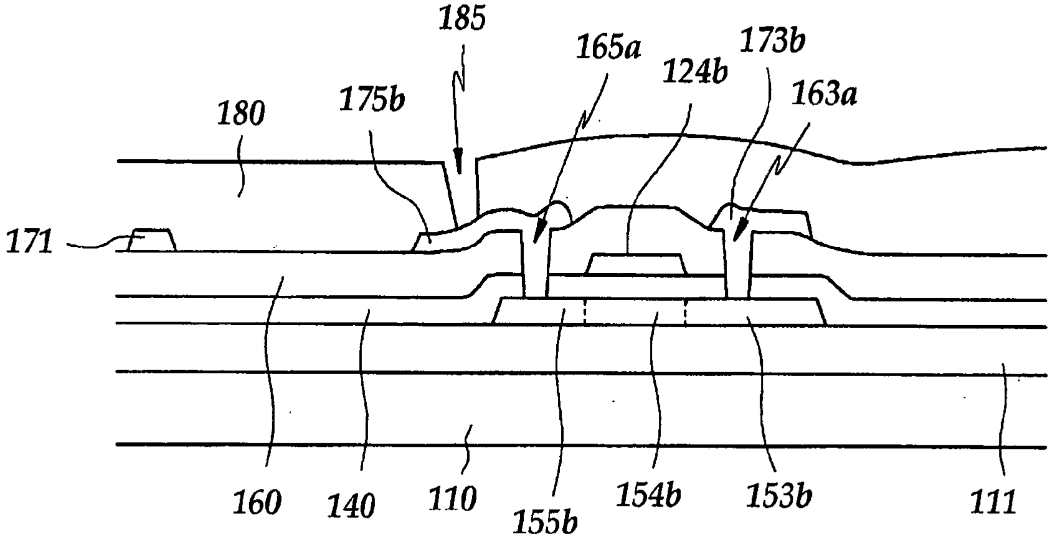

185
165a
173b
124b
163a
180
175b
171
160
140
110
155b
154b
153b
111

FIG. 16

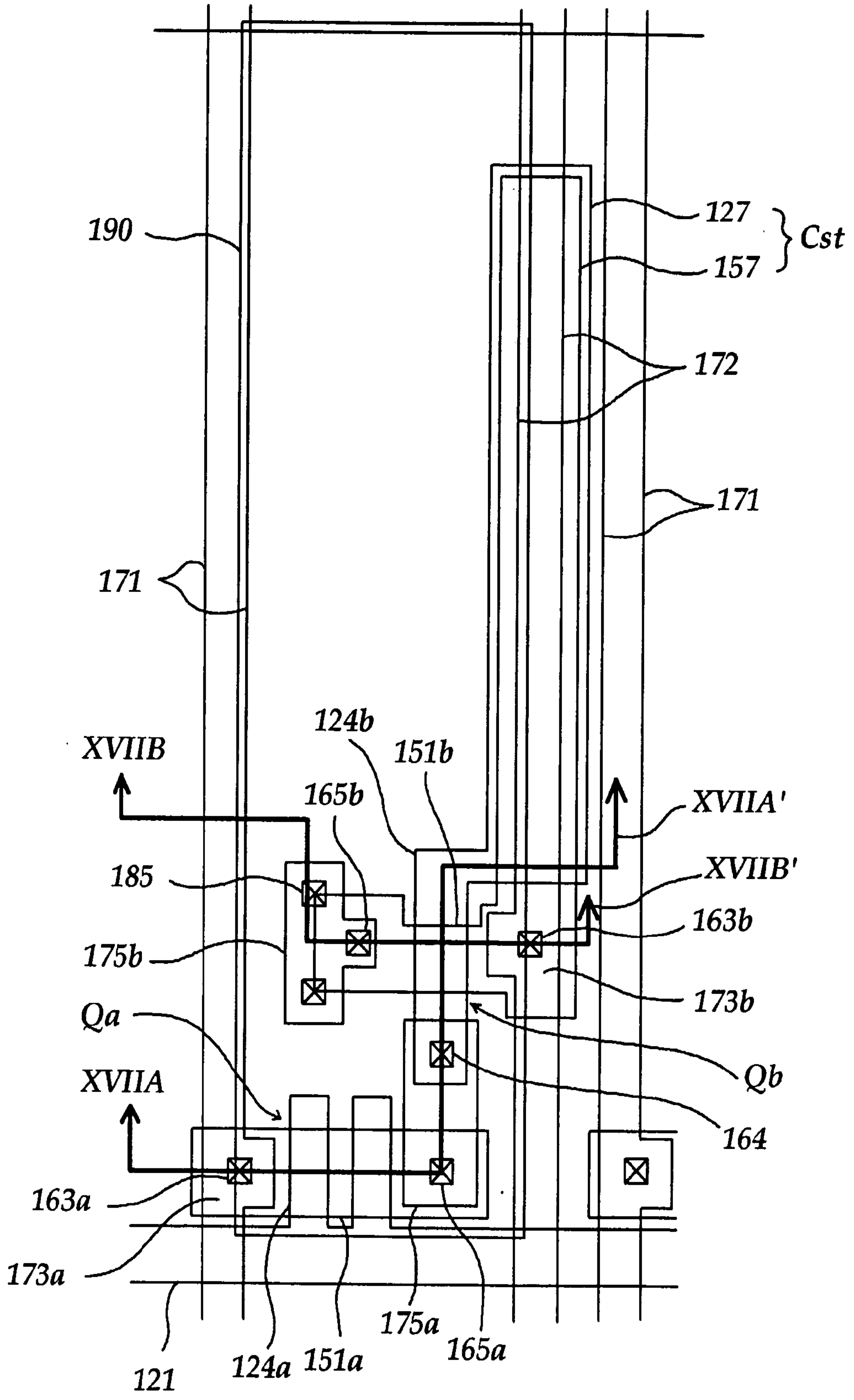

190
127
157
Cst
172
171
171
124b
151b
XVIIB
165b
XVIIA'
XVIIB'
185
163b
175b
173b
Qa
Qb
164
XVIIA
163a
173a
121
124a
151a
175a
165a

FIG. 17A

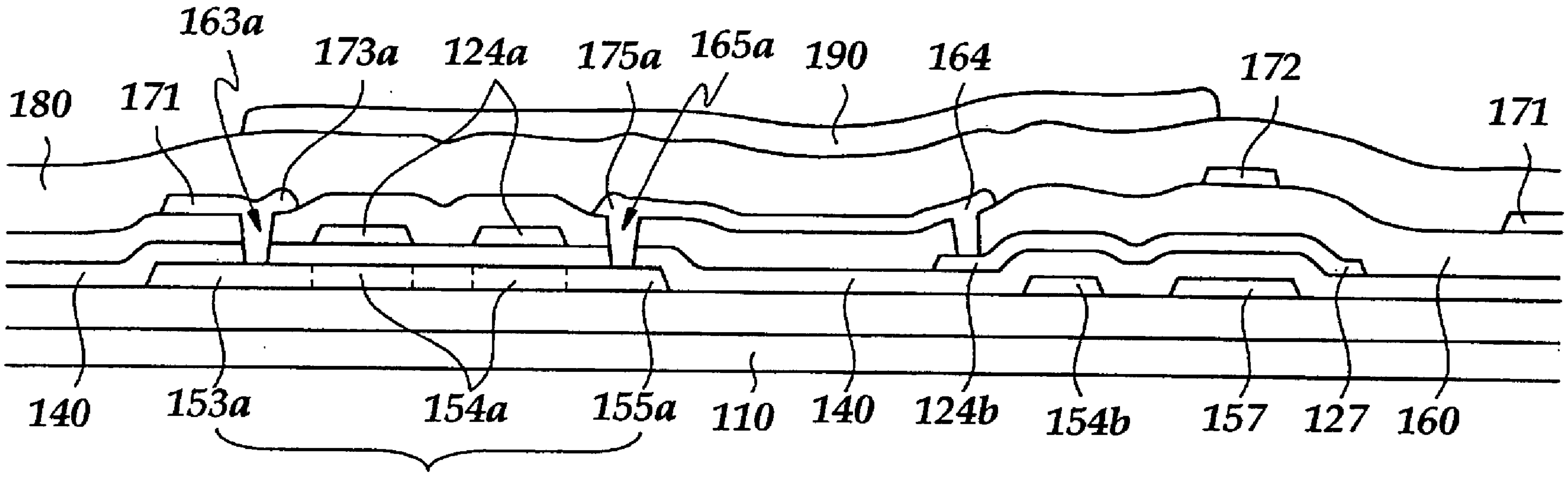

163a
173a
124a
175a
165a
190
164
172
180
171
171
140
153a
154a
155a
110
140
124b
154b
157
127
160

FIG. 17B

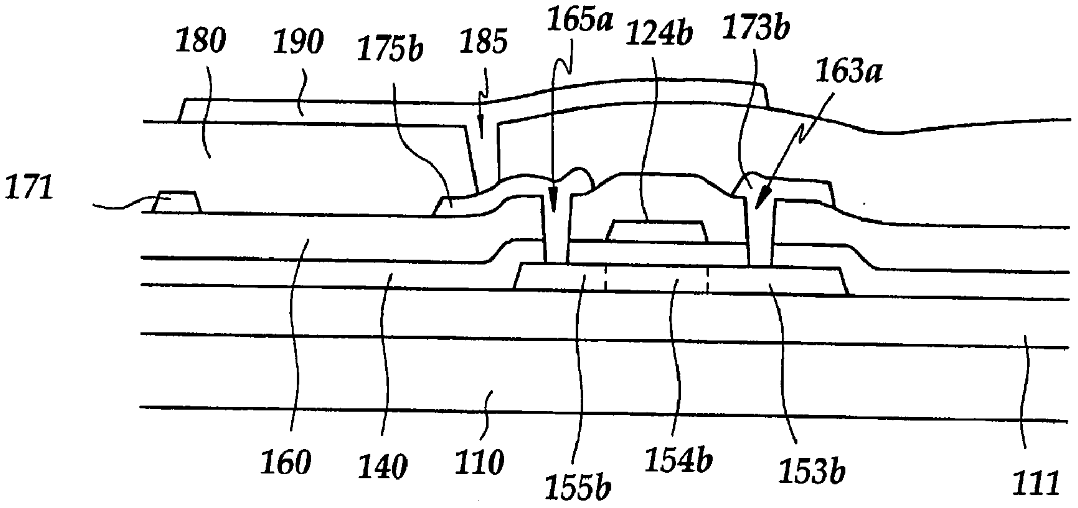

180
190
175b
185
165a
124b
173b
163a
171
160
140
110
155b
154b
153b
111

FIG. 18

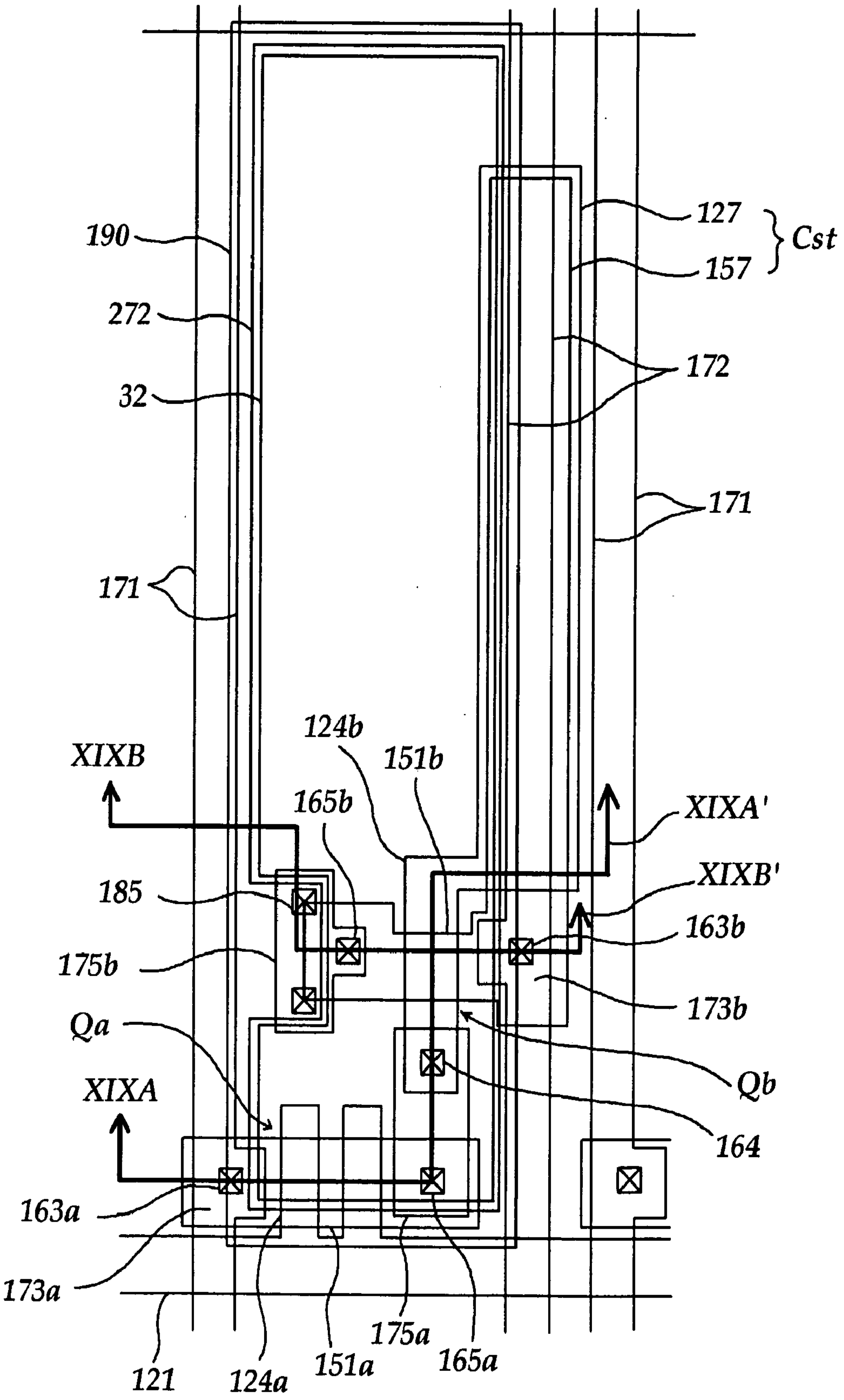
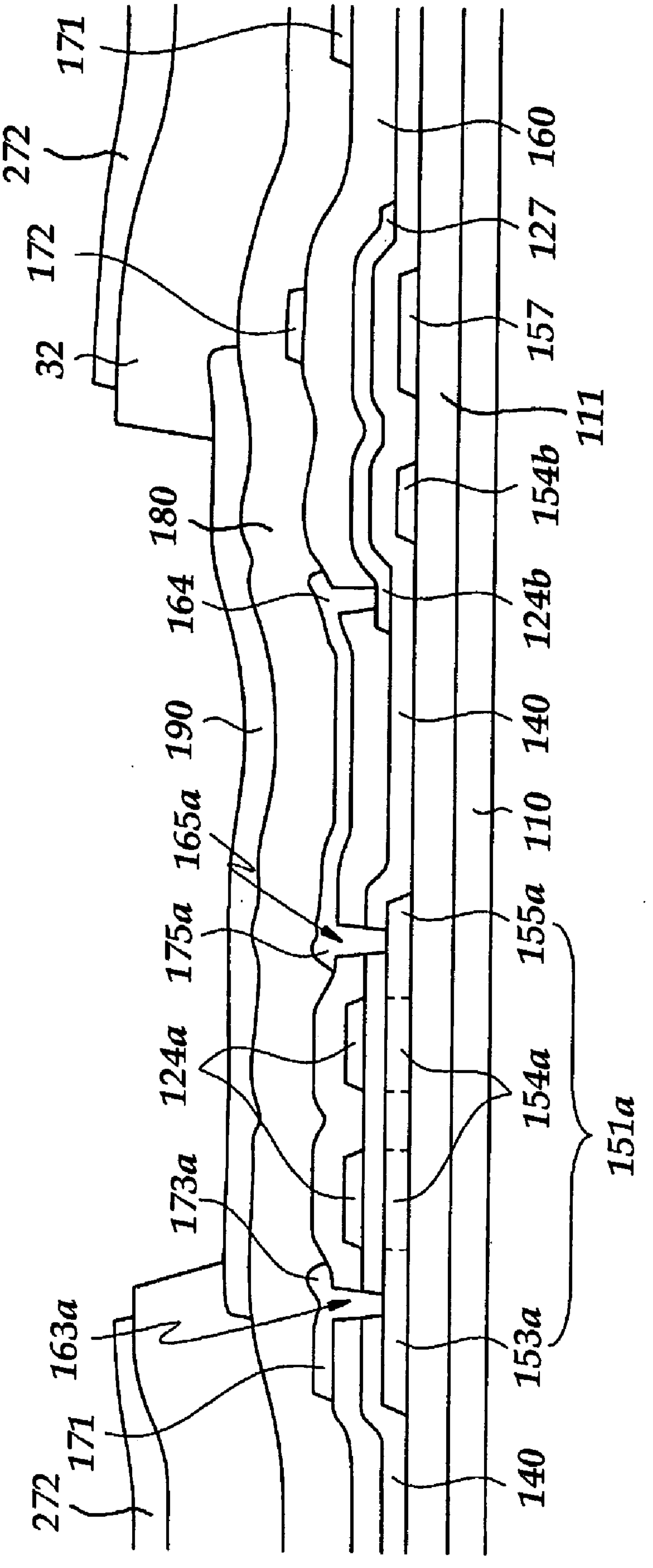

190
272
32
171
127
157
Cst
172
171
124b
151b
XIXB
165b
XIXA'
XIXB'
185
163b
175b
173b
Qa
Qb
XIXA
164
163a
173a
121
124a
151a
175a
165a

FIG. 19A


171
272
172
32
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164
190
165a
175a
124a
173a
163a
171
272
160
127
157
111
154b
124b
140
110
155a
154a
151a
153a
140

FIG. 19B

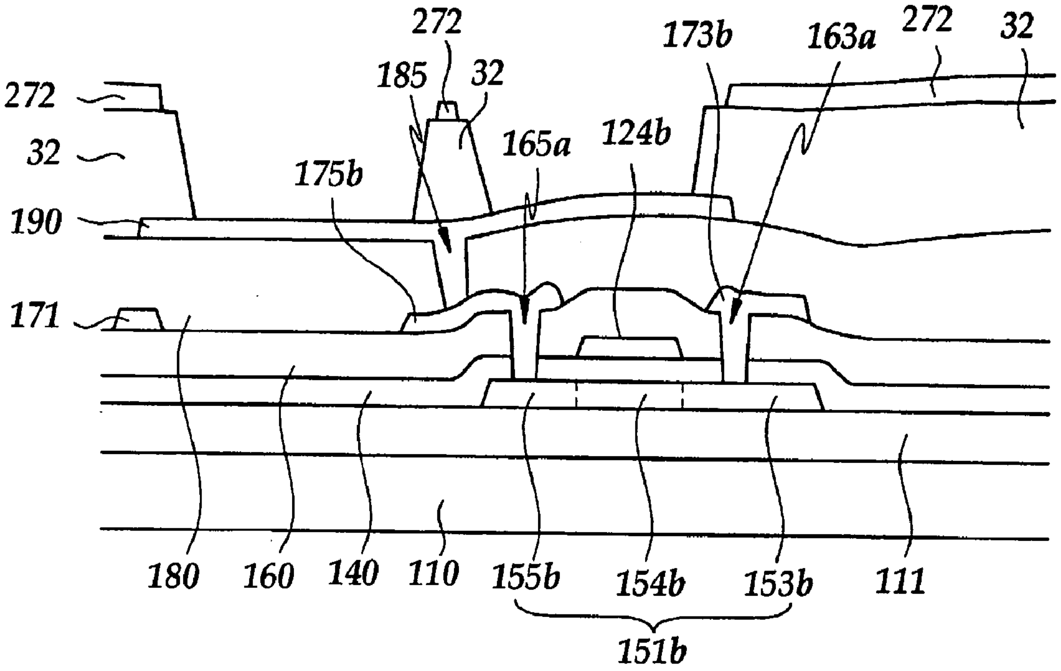

272
185
32
173b
163a
272
32
272
32
165a
124b
175b
190
171
180
160
140
110
155b
154b
153b
111
151b

FIG. 20A

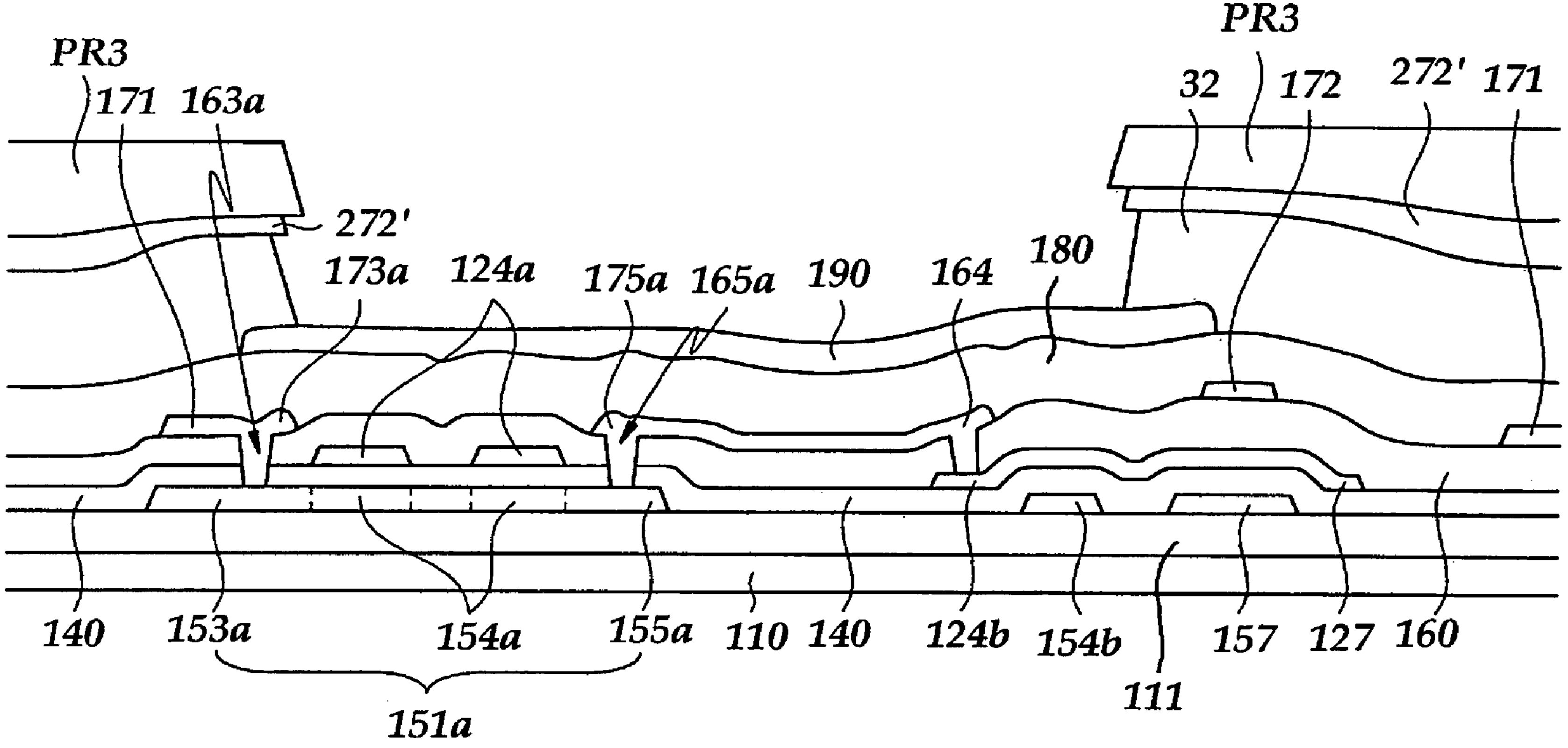

PR3
171
163a
272'
173a
124a
175a
165a
190
164
180
PR3
32
172
272'
171
140
153a
154a
155a
151a
110
140
124b
154b
111
157
127
160

FIG. 20B

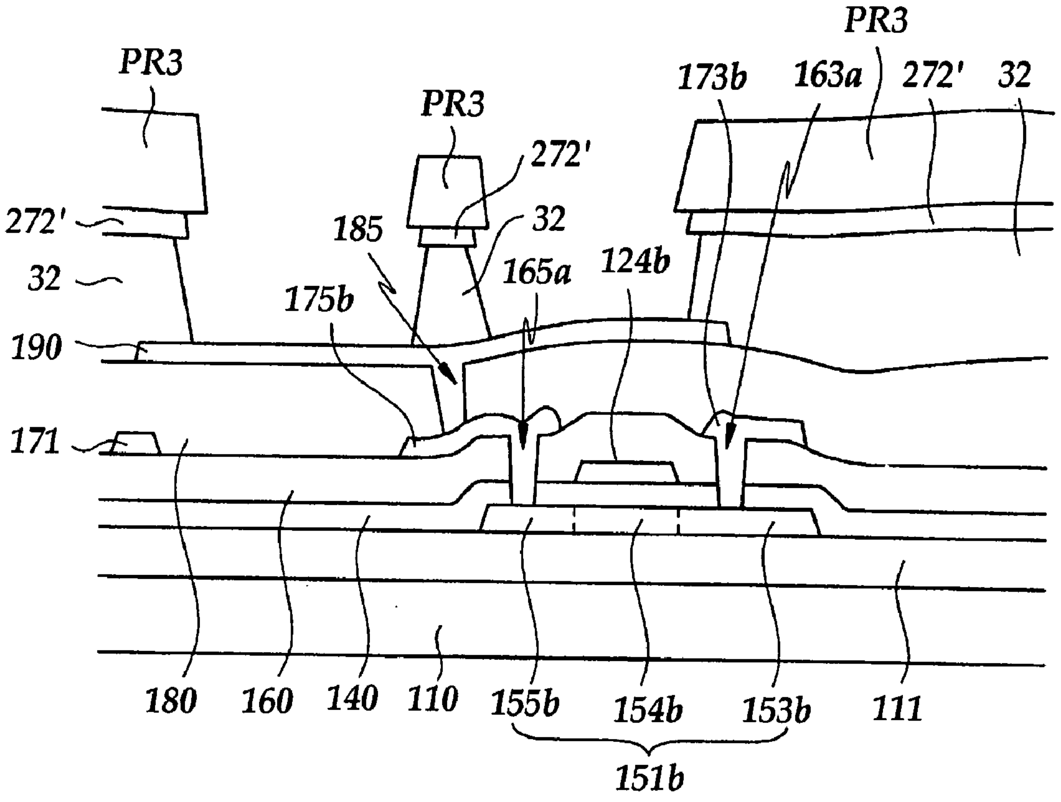

PR3
PR3
PR3
173b
163a
272'
32
272'
272'
32
32
185
165a
124b
175b
190
171
180
160
140
110
155b
154b
153b
111
151b

FIG. 21A

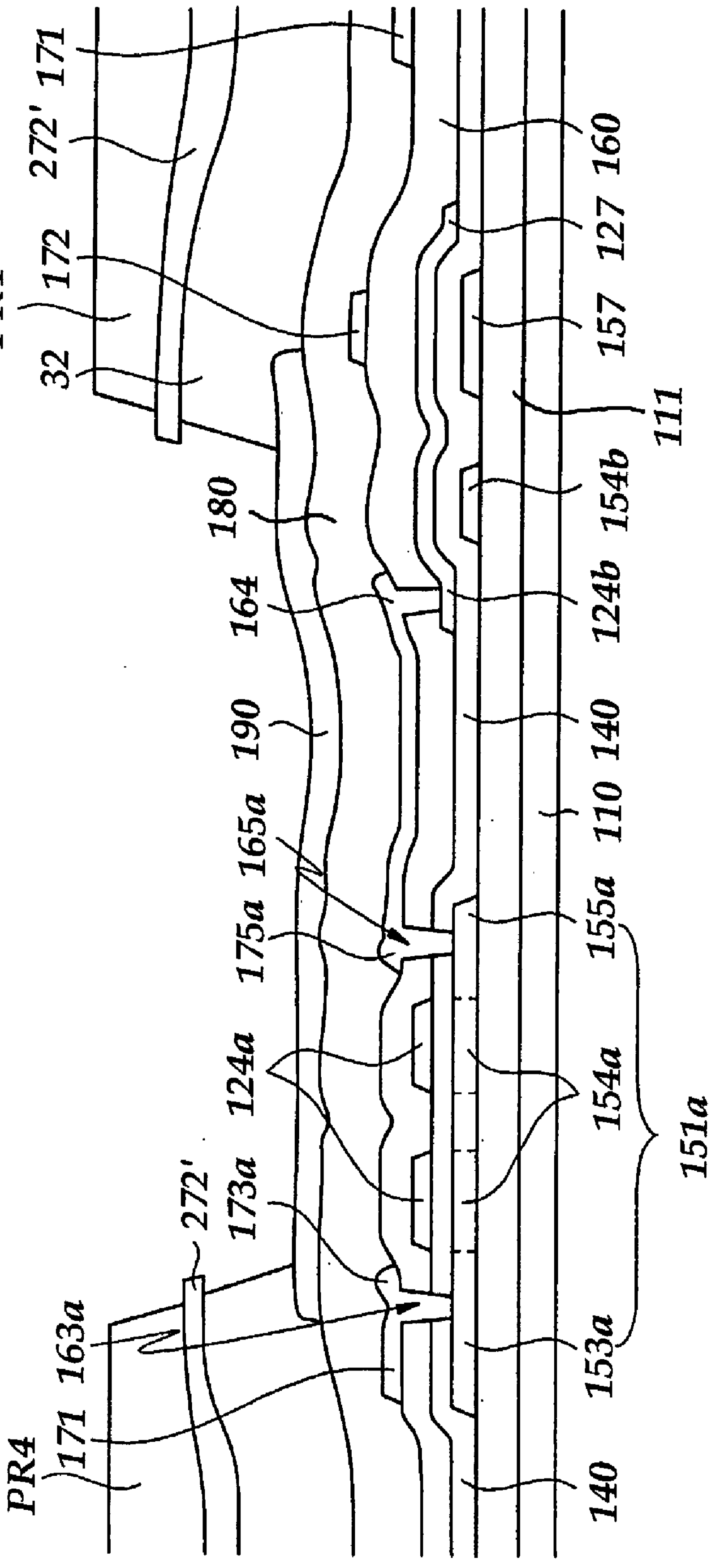

PR4
171
163a
272'
173a
124a
175a
165a
190
164
180
32
PR4
172
272'
171
140
153a
154a
151a
155a
110
140
124b
154b
111
157
127
160

FIG. 21B

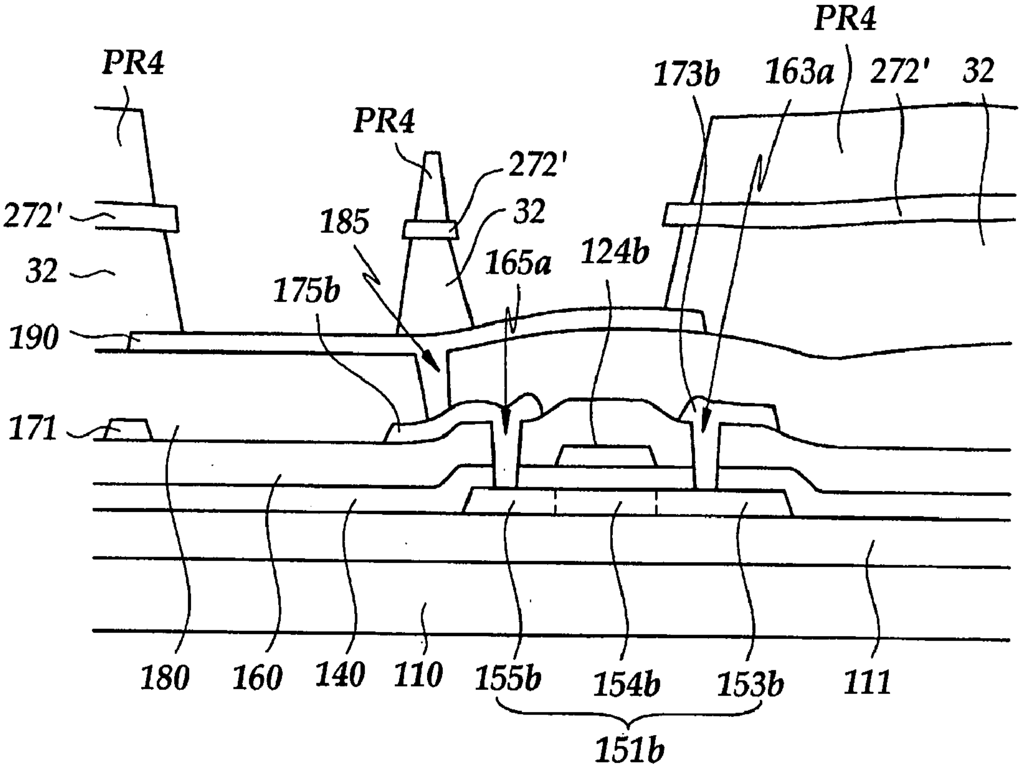

PR4
PR4
PR4
173b
163a
272'
32
272'
272'
32
185
32
165a
124b
175b
190
171
180
160
140
110
155b
154b
153b
111
151b

FIG. 22A

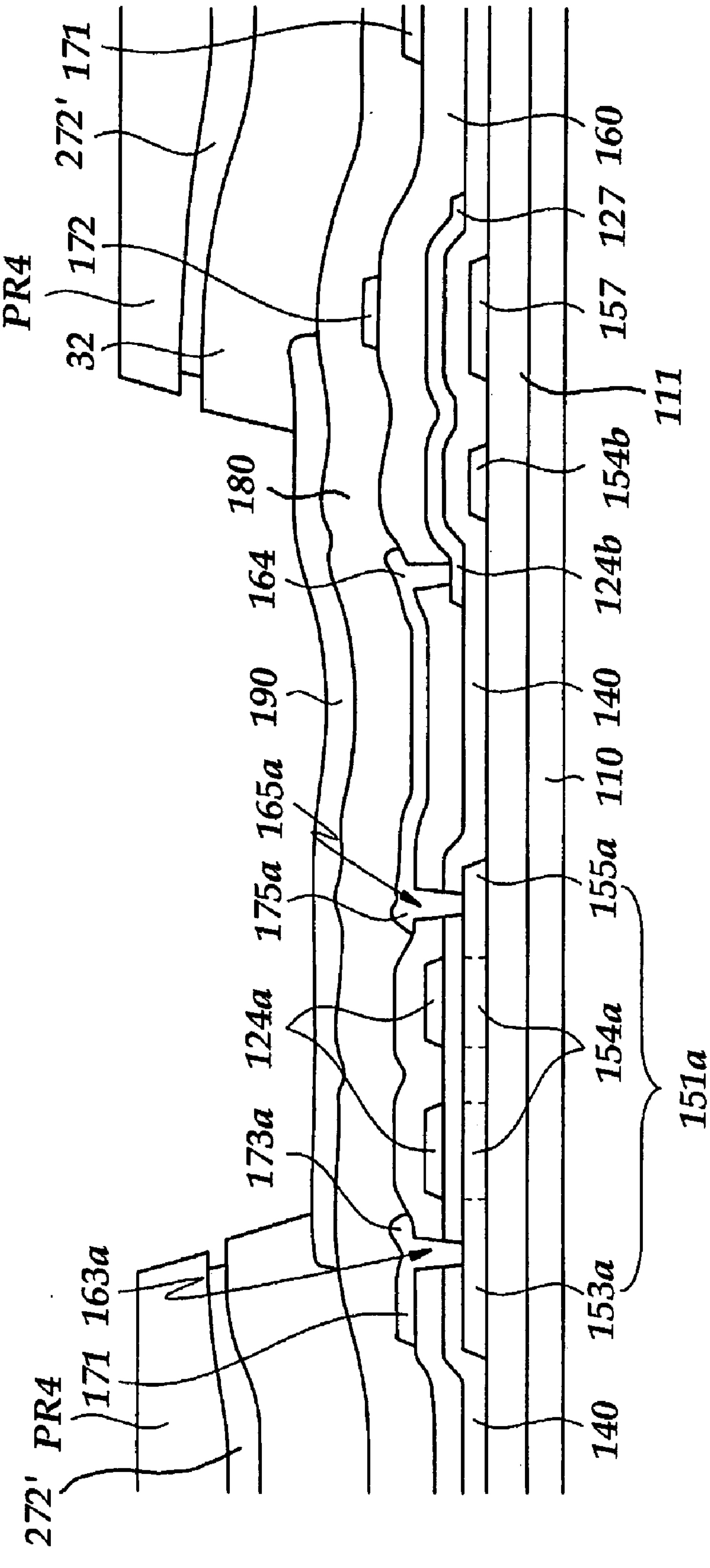

272'
PR4
171
163a
173a
124a
175a
165a
190
164
180
32
PR4
172
272'
171
140
153a
154a
151a
155a
110
140
124b
154b
111
157
127
160

FIG. 22B

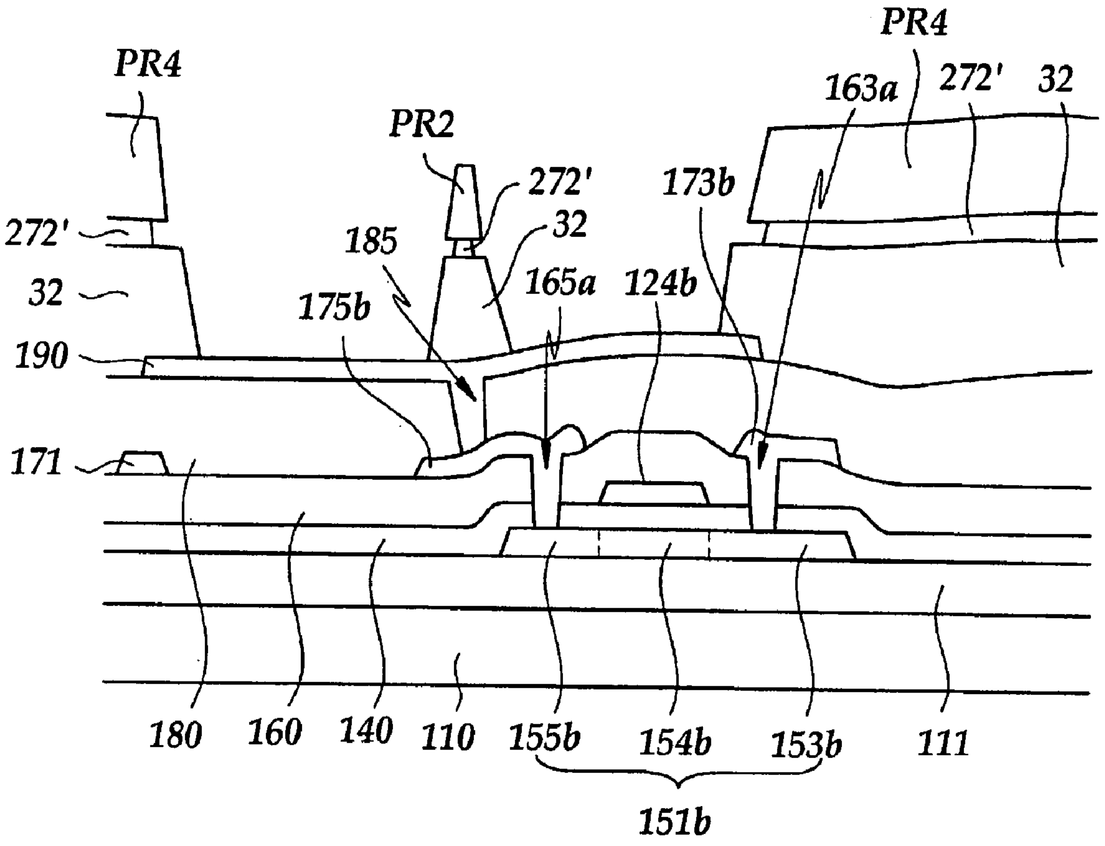

PR4
PR4
163a
272'
32
PR2
272'
173b
272'
32
185
165a
124b
32
175b
190
171
180
160
140
110
155b
154b
153b
111
151b

FIG. 23

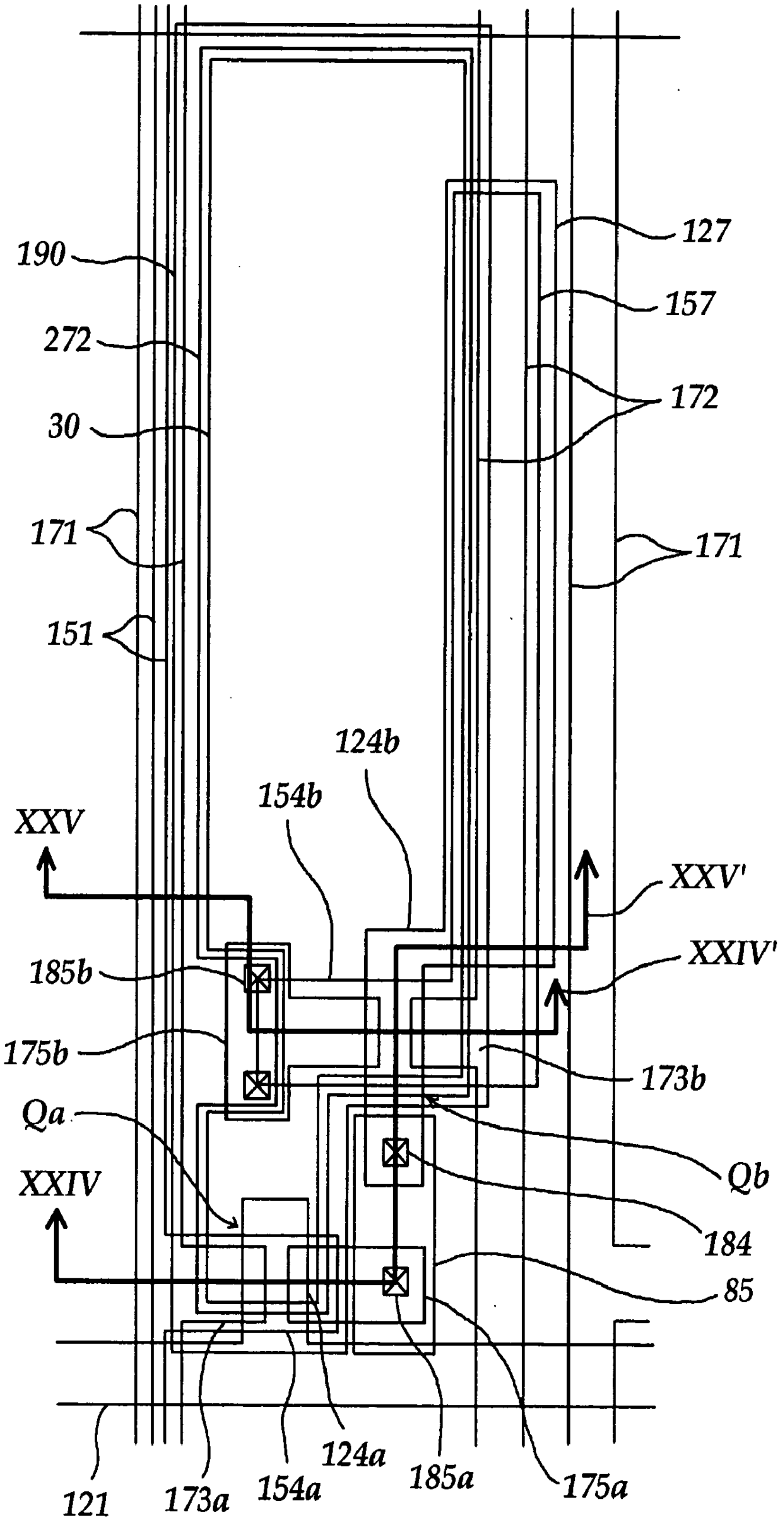

190
272
30
171
151
127
157
172
171
124b
154b
XXV
XXV'
XXIV'
185b
175b
173b
Qa
Qb
XXIV
184
85
121
173a
154a
124a
185a
175a

FIG. 24

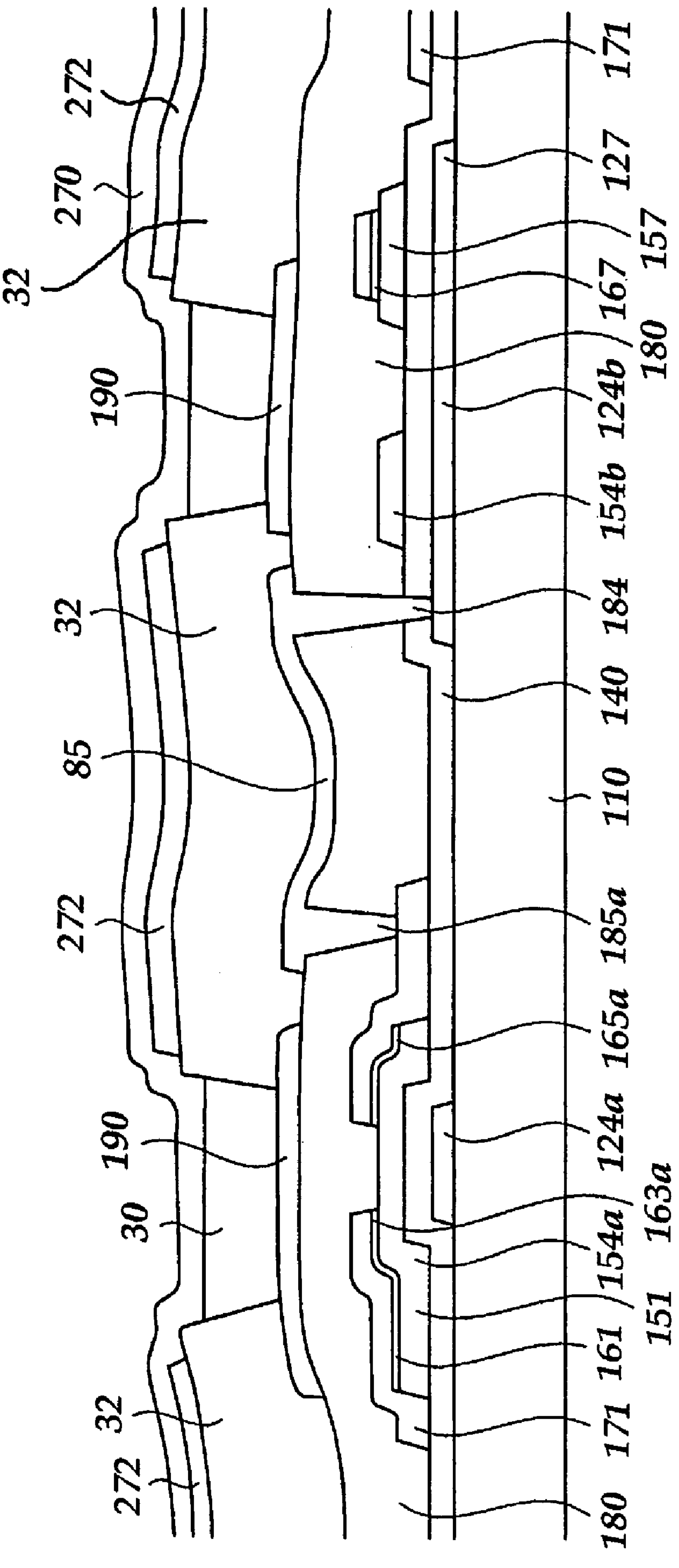

272
270
32
190
32
85
272
190
30
32
272
171
127
157
167
180
124b
154b
184
140
110
185a
165a
124a
163a
154a
151
161
171
180

FIG. 25

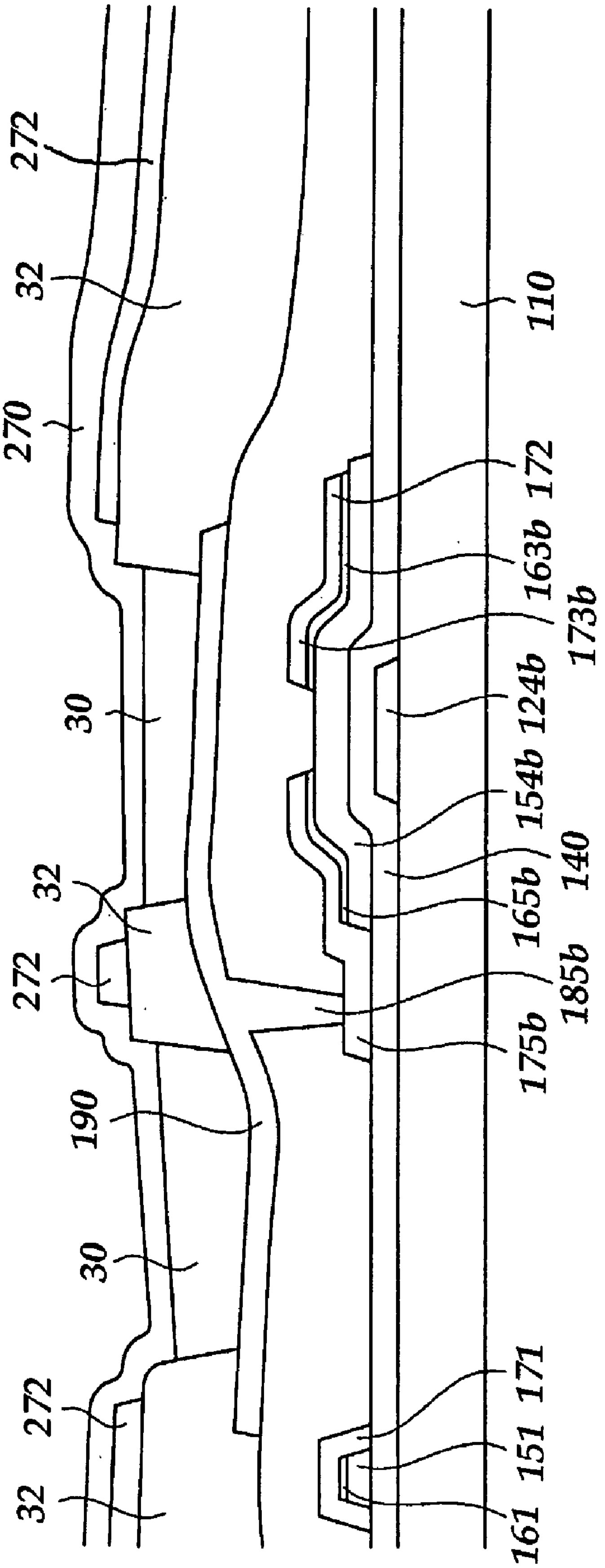

32
272
30
190
272
32
30
270
32
272
161
151
171
175b
185b
165b
140
154b
124b
173b
163b
172
110

FIG. 26

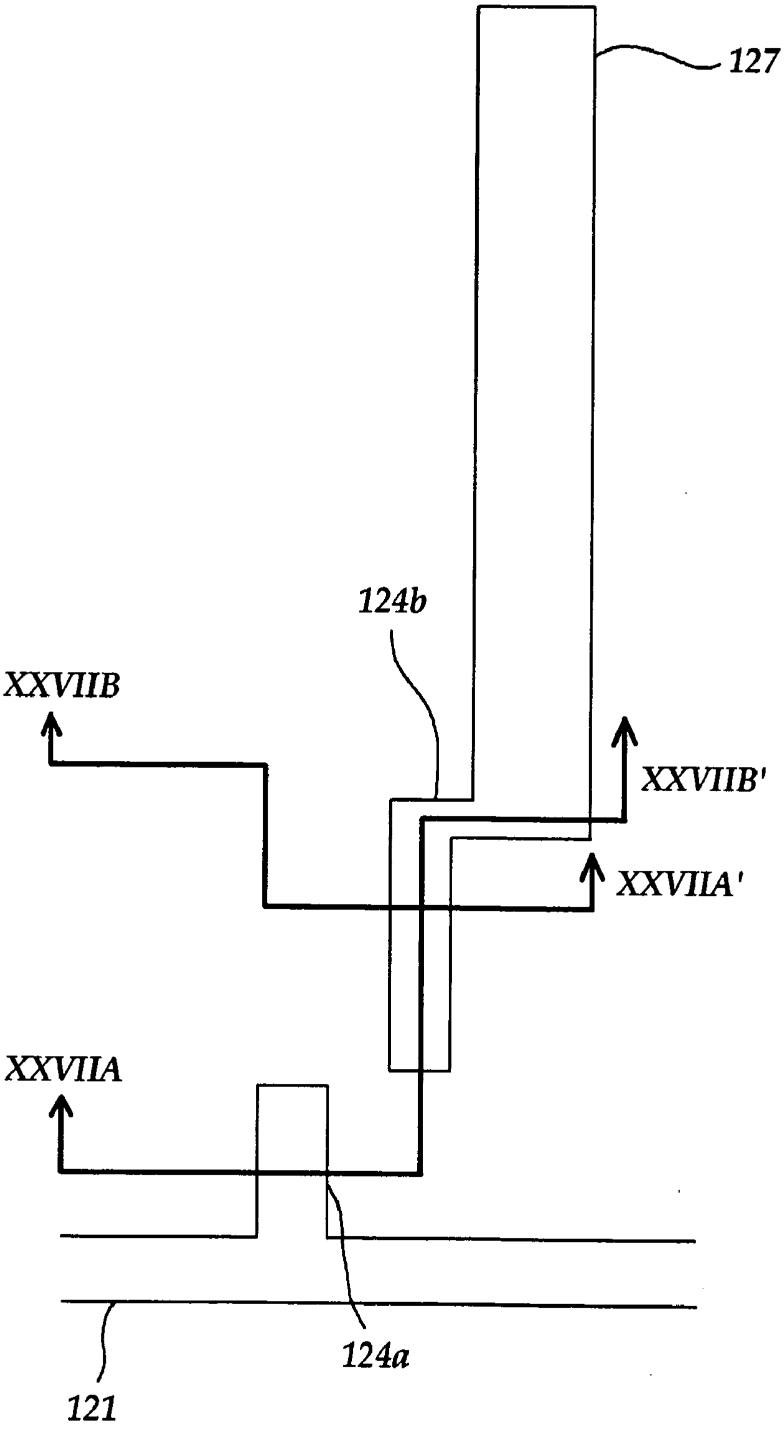
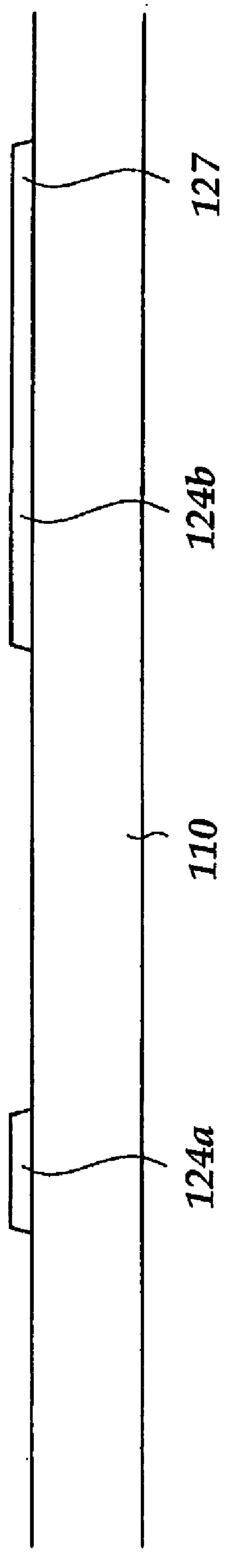


FIG. 27A



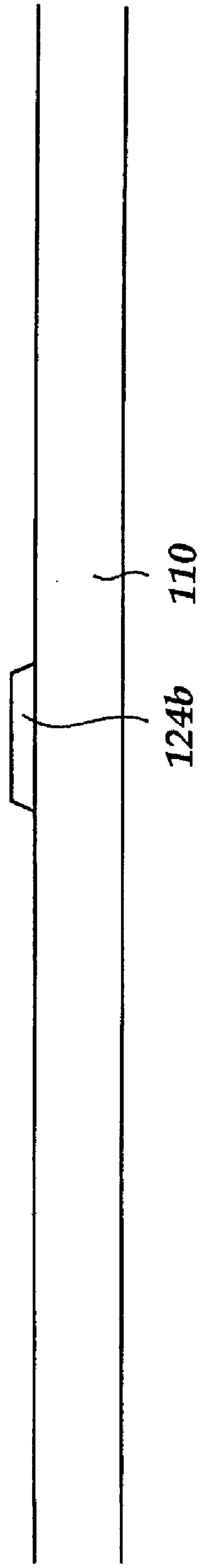


FIG. 27B

FIG. 28

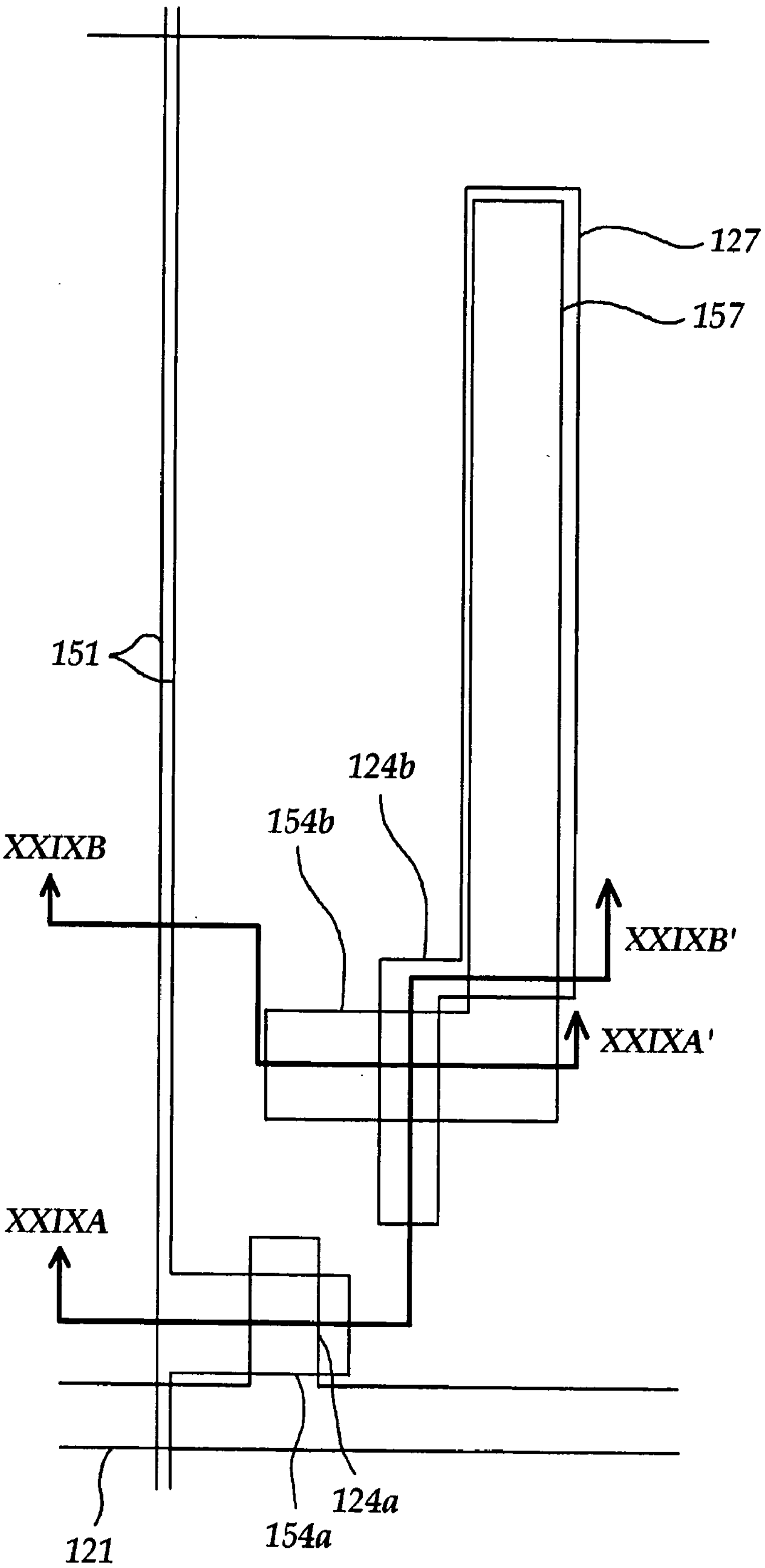


FIG. 29A

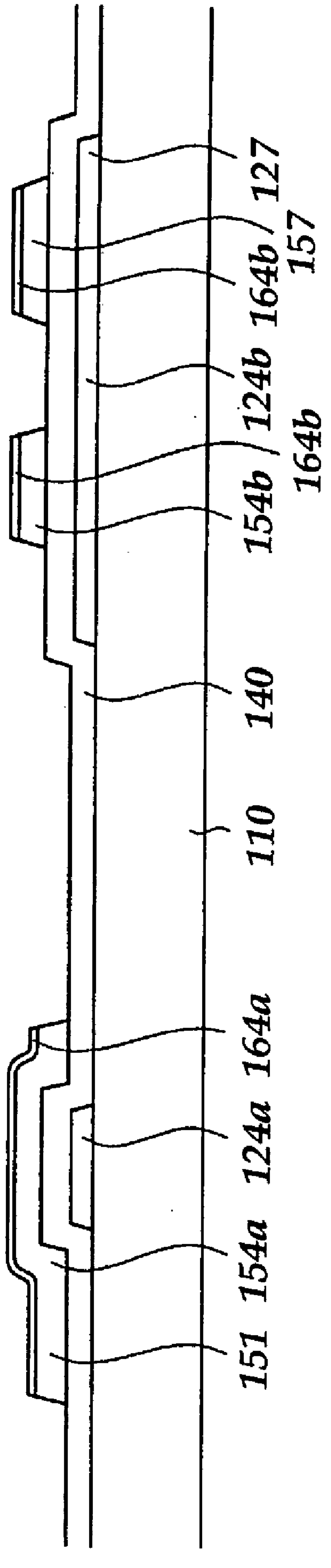


FIG. 29B

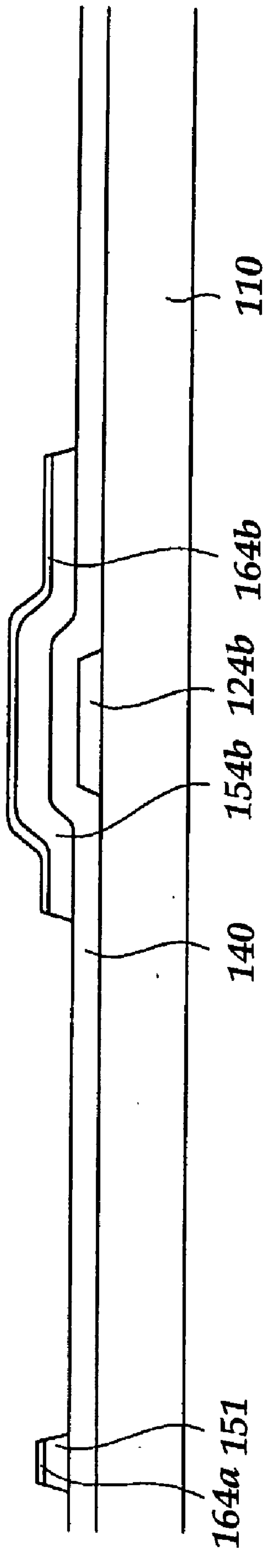


FIG. 30

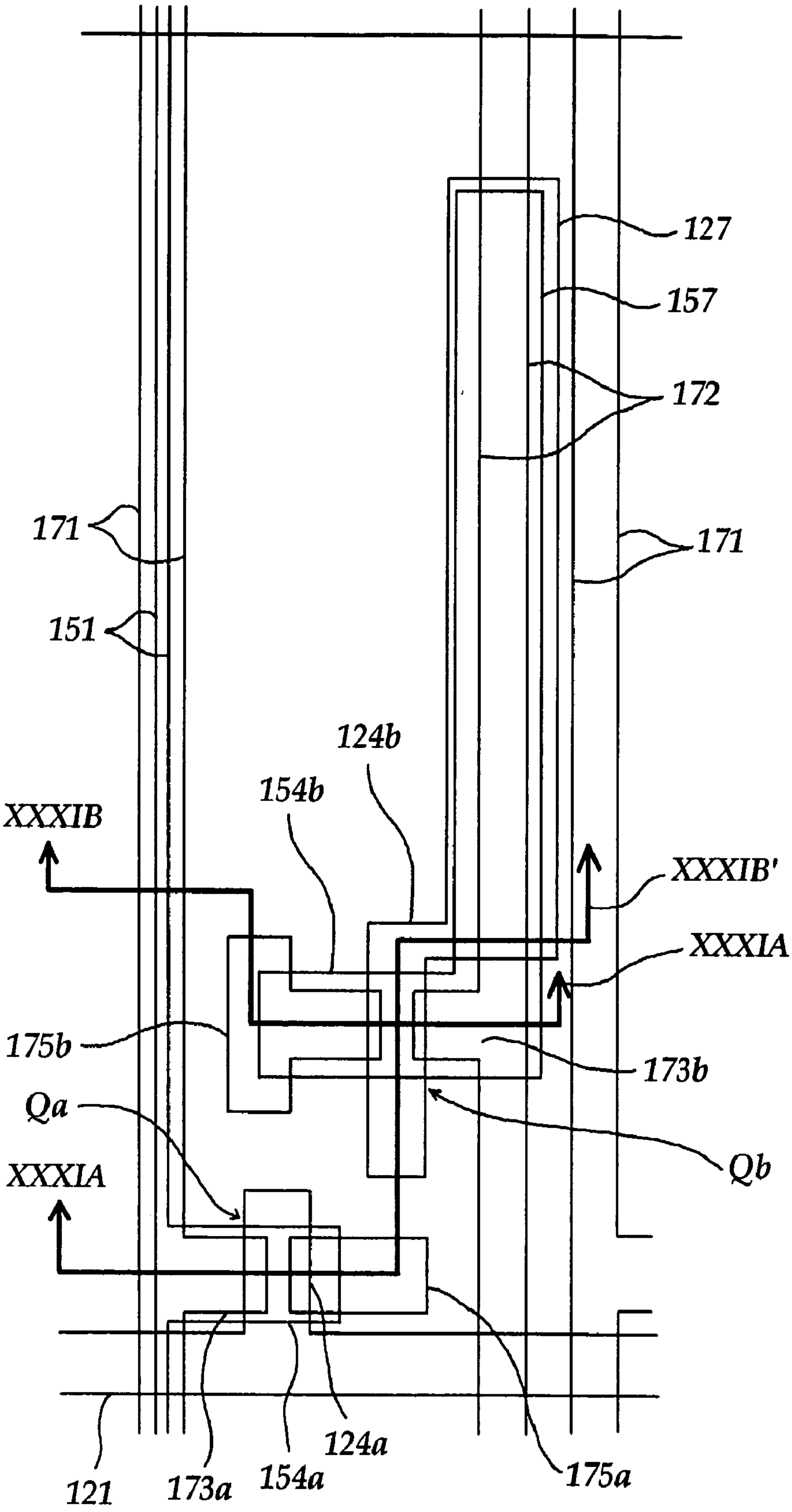

127
157
172
171
171
151
124b
154b
XXXIB
XXXIB'
XXXIA'
175b
173b
Qa
Qb
XXXIA
124a
121
173a
154a
175a

FIG. 31A

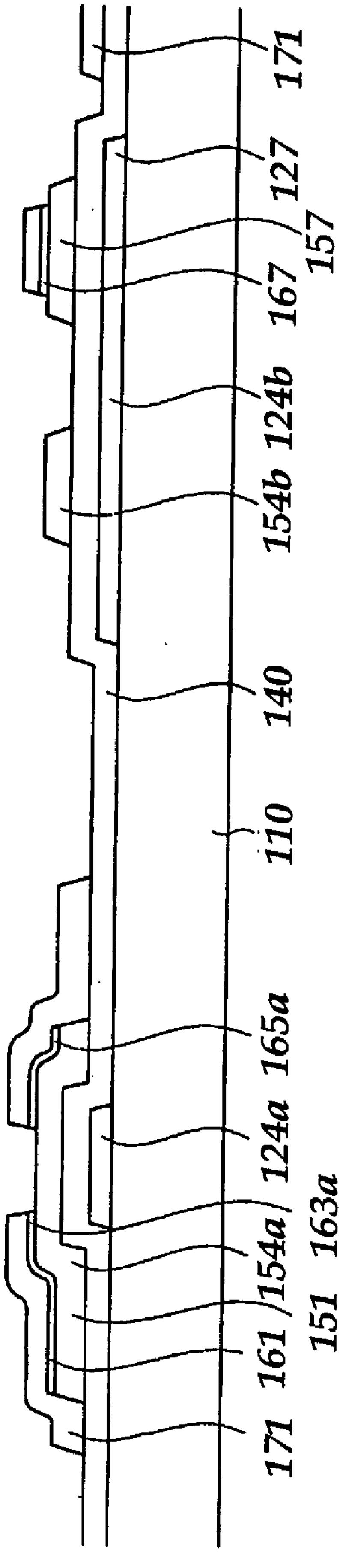

171
161
151
154a
163a
124a
165a
110
140
154b
124b
167
157
127
171

FIG. 31B

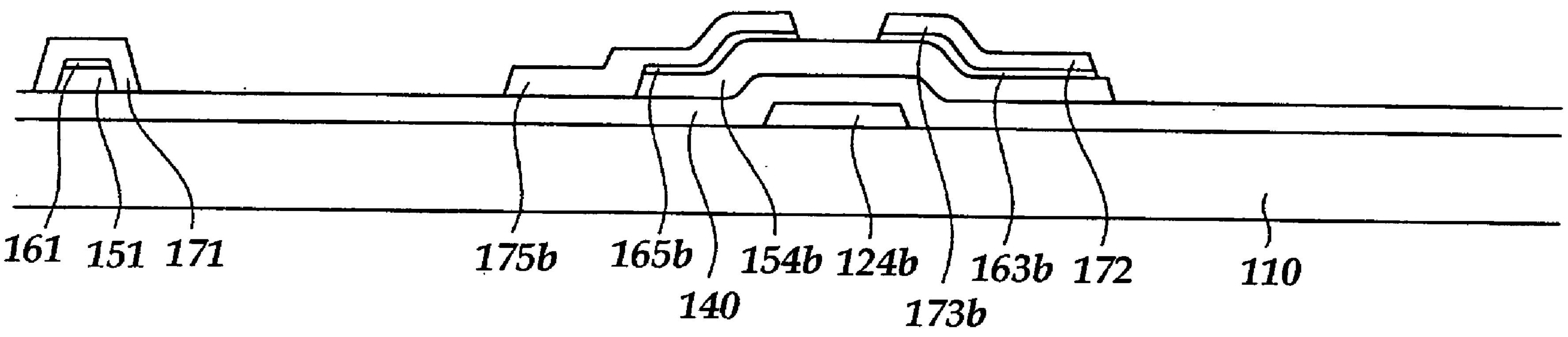


FIG. 32

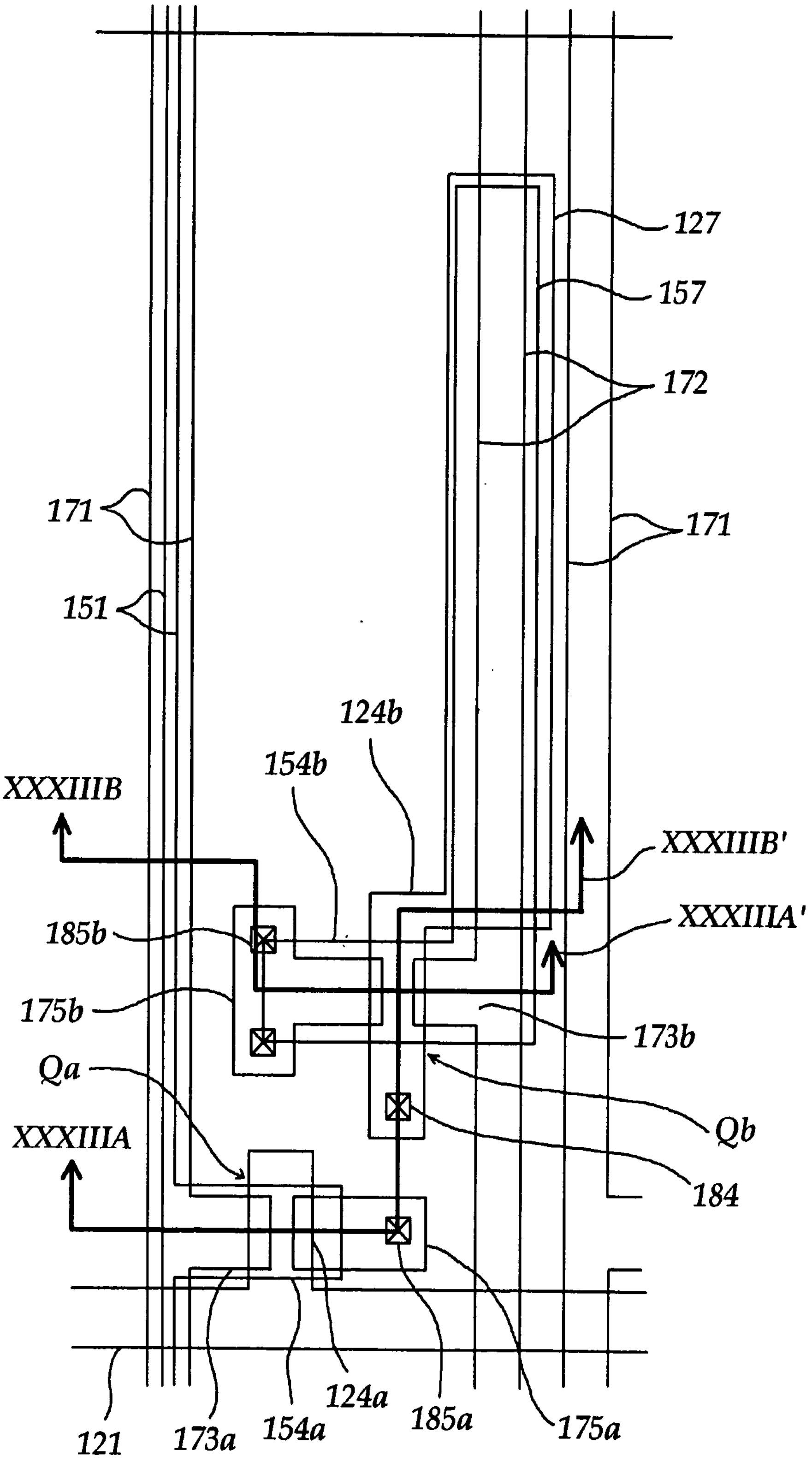
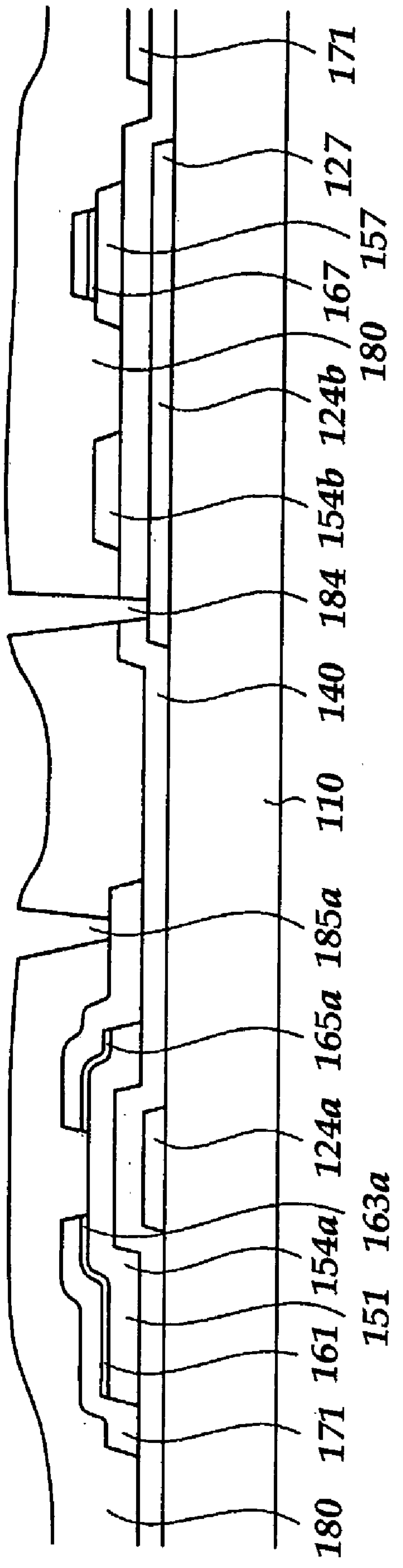

127
157
172
171
171
151
124b
154b
XXXIIIB
XXXIIIB'
XXXIIIA'
185b
175b
173b
Qa
Qb
XXXIIIA
184
121
173a
154a
124a
185a
175a

FIG. 33A


180
171
161
151
154a
163a
124a
165a
185a
110
140
184
154b
124b
180
167
157
127
171

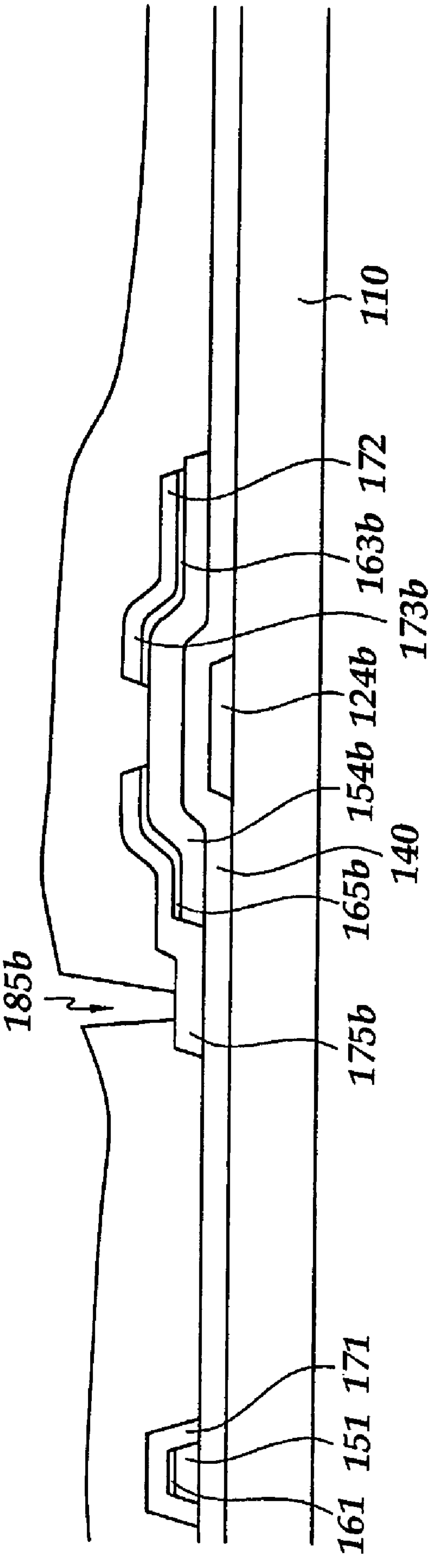


FIG. 33B

FIG. 34

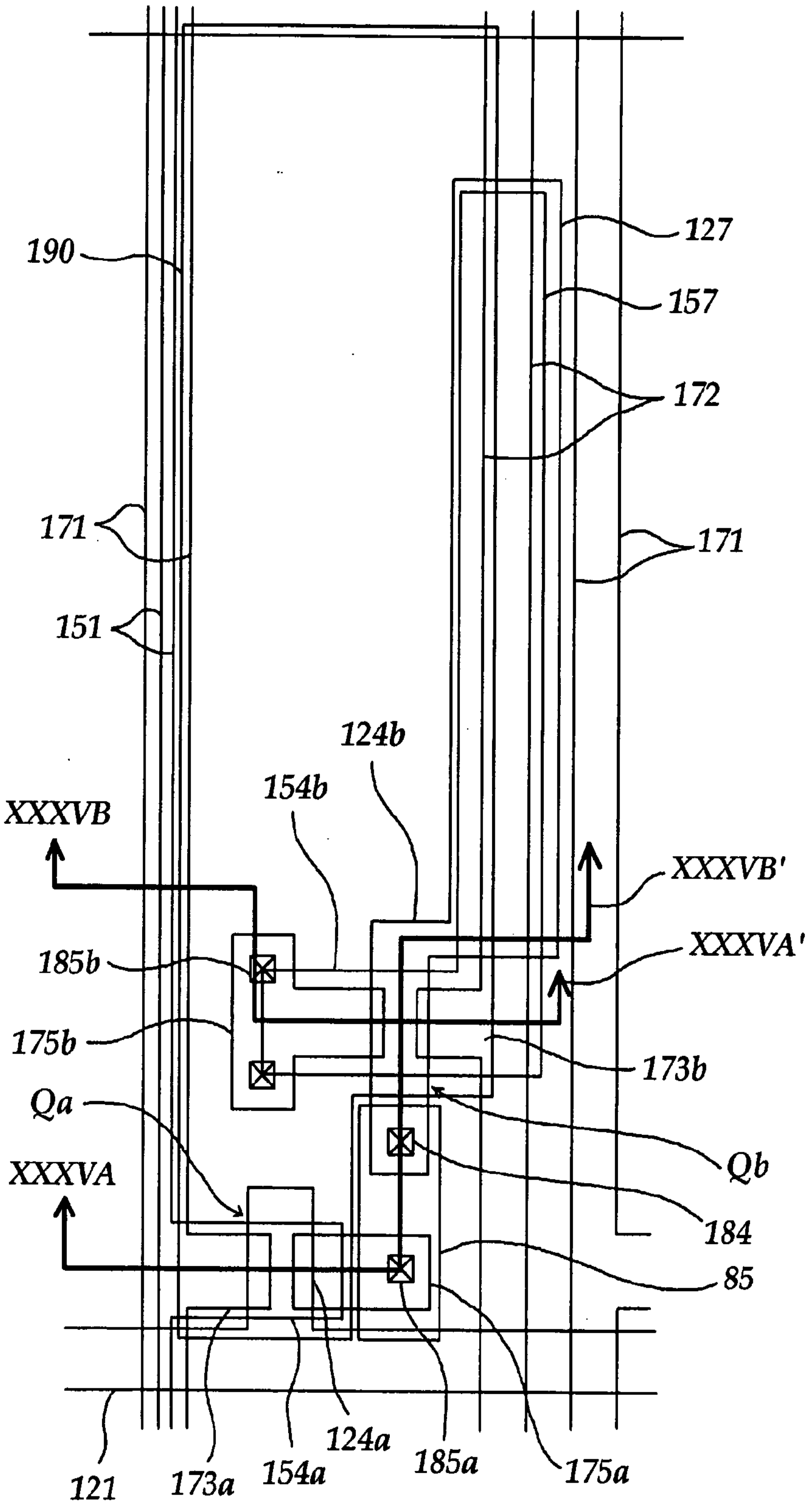

190
127
157
172
171
151
171
124b
154b
XXXVB
XXXVB'
XXXVA'
185b
175b
173b
Qa
Qb
XXXVA
184
85
121
173a
154a
124a
185a
175a

FIG. 35A

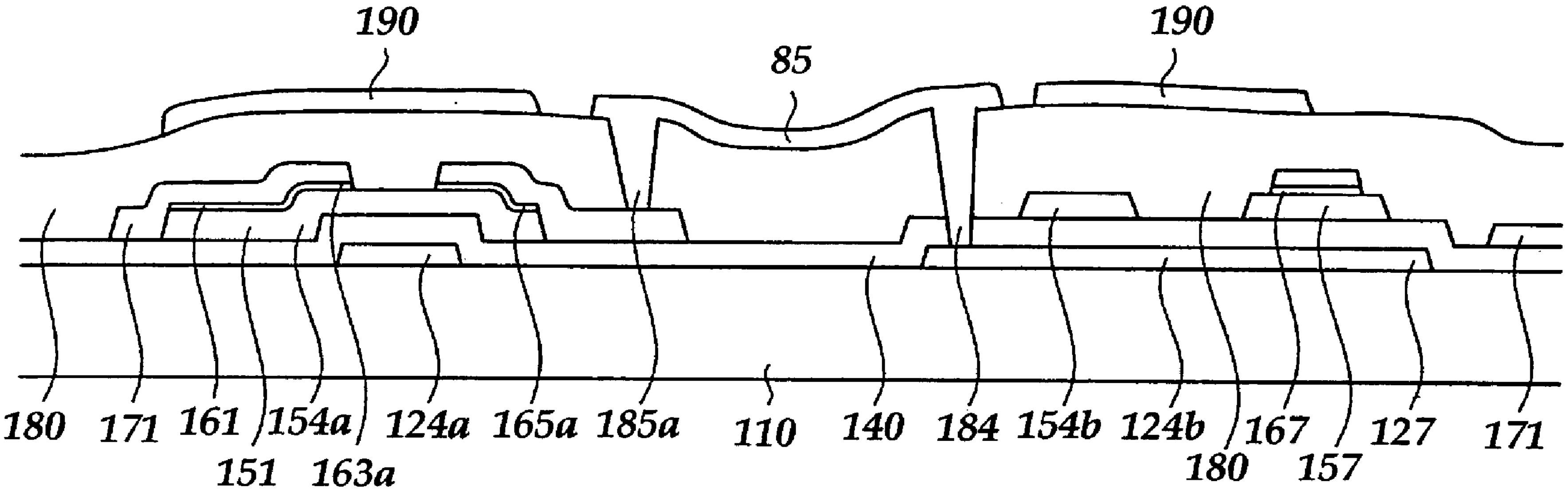

190
85
190
180
171
161
151
154a
163a
124a
165a
185a
110
140
184
154b
124b
180
167
157
127
171

FIG. 35B

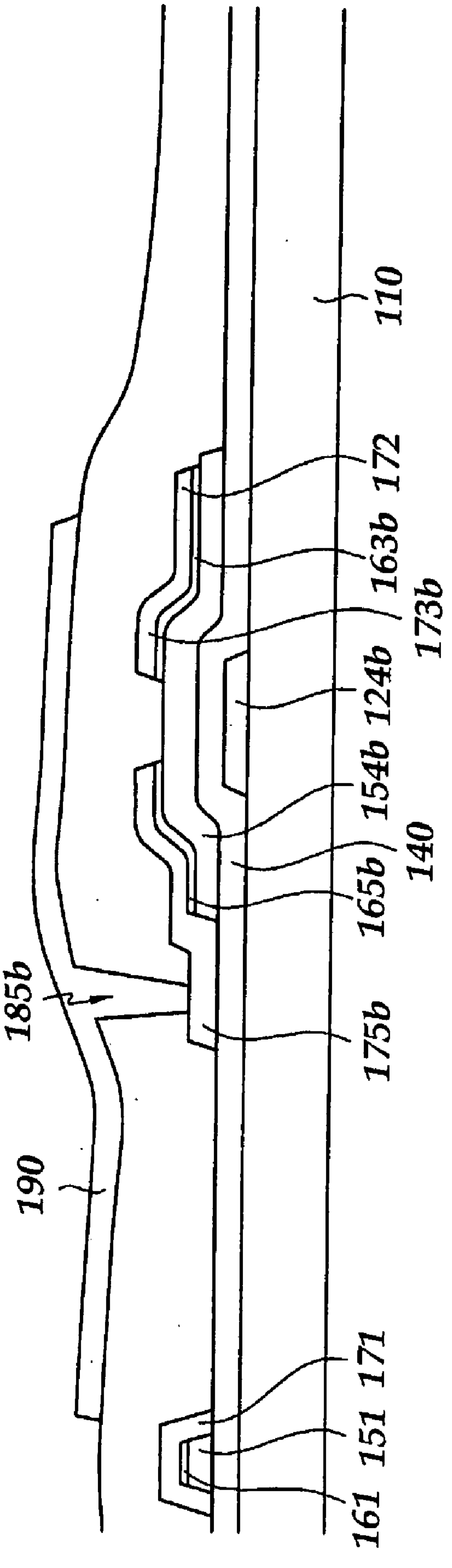


FIG. 36

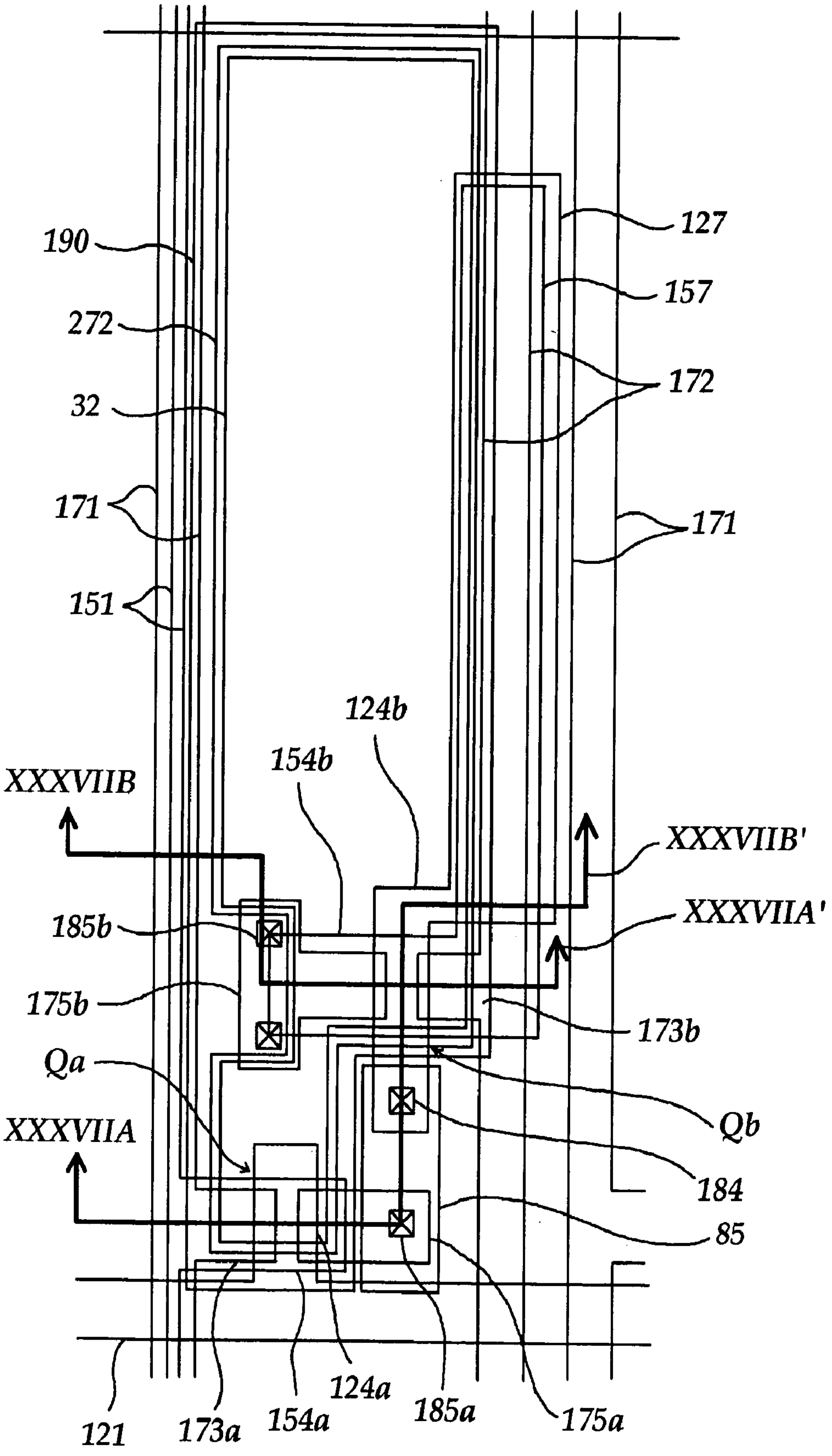

190
272
32
171
151
127
157
172
171
124b
154b
XXXVIIB
XXXVIIB'
XXXVIIA'
185b
175b
173b
Qa
Qb
XXXVIIA
184
85
121
173a
154a
124a
185a
175a

FIG. 37A

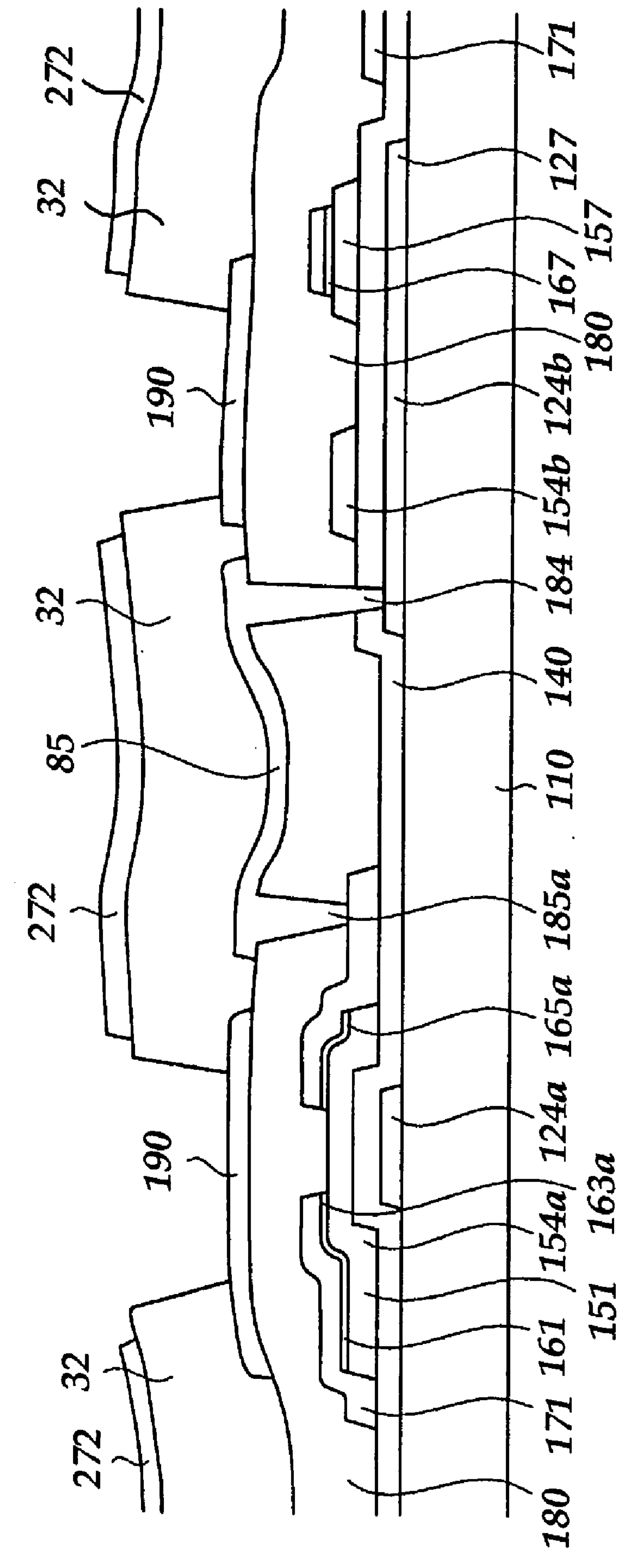
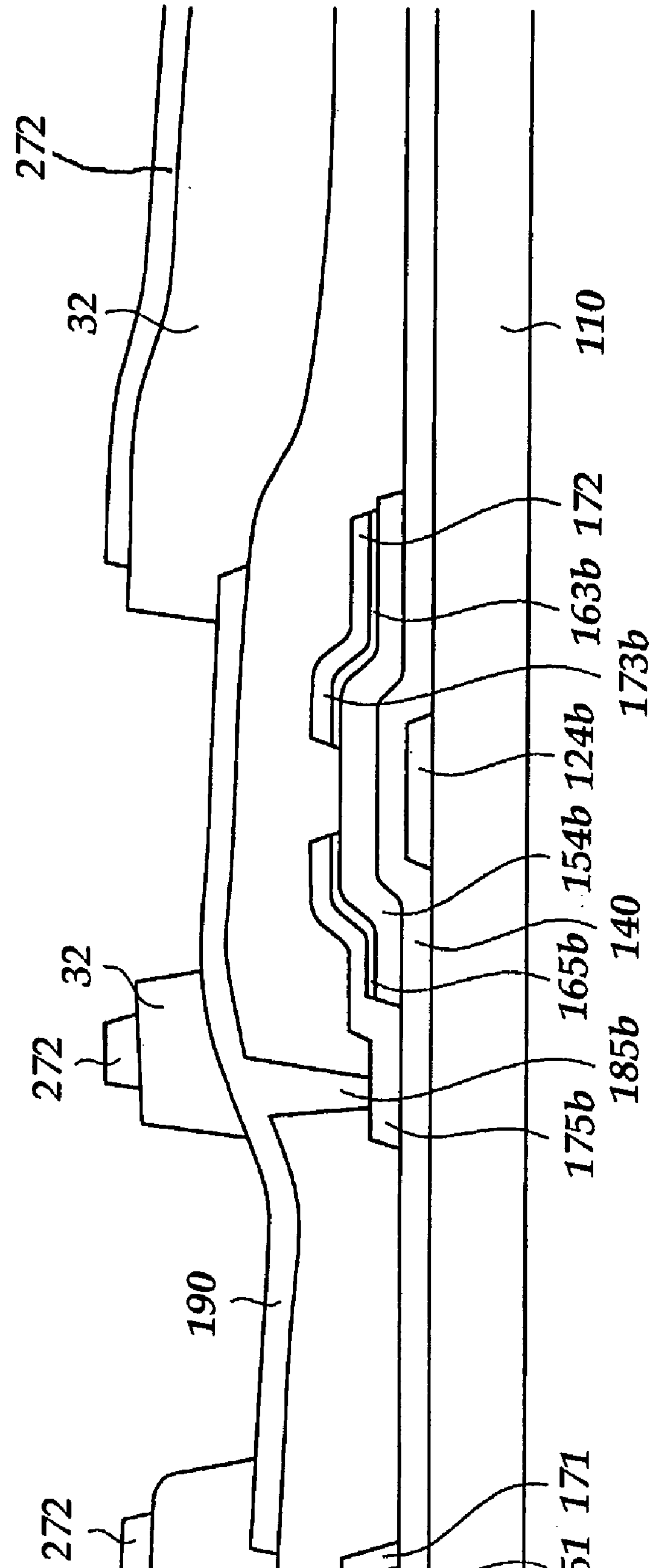

272
32
190
272
85
32
190
32
272
180
171
161
151
154a
163a
124a
165a
185a
110
140
184
154b
124b
180
167
157
127
171

FIG. 37B


32
272
190
32
272
161
151
171
175b
185b
165b
140
154b
124b
173b
163b
172
110
32
272

ORGANIC LIGHT EMITTING DISPLAY AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

[0001] (a) Field of the Invention

[0002] The present invention relates to an organic light emitting display and a manufacturing method thereof.

[0003] (b) Description of Related Art

[0004] An organic light emitting display (OLED) is a self emissive display device, which displays images by exciting an emissive organic material to emit light. The OLED includes an anode (hole injection electrode), a cathode (electron injection electrode), and an organic light emission layer interposed therebetween. When the holes and the electrons are injected into the light emission layer, they are recombined and pair annihilated with emitting light. The light emission layer further includes an electron transport layer (ETL) and a hole transport layer (HTL) as well as an electron injecting layer (EIL) and a hole injecting layer (HIL) for enhancing the light emission. Each pixel of the OLED includes two TFTs, i.e., a switching TFT and a driving TFT. The current for light emission is driven by the driving TFT and the mount of the current driven the driving TFT is controlled by the data signals from the switching TFT.

[0005] A plurality of pixels of the OLED, each including an anode, a cathode, and a light emission layer, are arranged in a matrix and driven in passive matrix (or simple matrix) addressing or active matrix addressing.

[0006] The passive matrix type OLED includes a plurality of anode lines, a plurality of cathode lines intersecting the anode lines, and a plurality of pixels, each including a light emission layer. The selection of one of the anode lines and one of the cathode lines cause light emission of a pixel located at the intersection of the selected signal lines.

[0007] The active matrix type OLED includes a plurality of pixels, each including a switching transistor, a driving transistor, and a storage capacitor as well as an anode, a cathode, and a light emission layer. The OLED further includes a plurality of gate lines transmitting gate signals and a plurality of data lines transmitting data voltages. The switching transistor is connected to one of the gate lines and one of the data lines and transmits the data voltage from the data line in response to the gate signal. The driving transistor receives the data voltage from the switching transistor and drives a current having a magnitude determined depending on the difference between the data voltage and a predetermined voltage such as a supply voltage. The current from the driving transistor enters the light emission layer to cause light emission having an intensity depending on the current. The storage capacitor is connected between the data voltage and the supply voltage to maintain their voltage difference. The gray scaling of the active matrix type OLED is accomplished by controlling the data voltages to adjust the current driven by the driving transistor. The color representation of the OLED is obtained by providing red, green and blue light emission layers.

[0008] In the meantime, the OLED is classified into top emission type and bottom emission type depending on the light emitting direction. The top emission type OLED includes a transparent cathode usually made of indium tin oxide (ITO) or indium zinc oxide (IZO) and an opaque anode, while the bottom emission type OLED includes an opaque cathode and a transparent anode. The relative positions of the anode and the cathode can be altered if required.

[0009] Since ITO and IZO have high resistivity, the top emission type OLED may add an auxiliary electrode having low resistivity to the cathode. However, the addition of the auxiliary electrode requires an additional lithography step that may complicate the manufacturing process and increase the manufacturing cost.

SUMMARY OF THE INVENTION

[0010] A motivation of the present invention is to solve the problems of conventional techniques.

[0011] An organic light emitting display is provided, which includes: a first electrode formed on a substrate; a partition having an opening exposing the first electrode at least in part; an auxiliary electrode formed on the partition and having substantially the same planar shape as the partition; an organic light emitting member formed on the first electrode and disposed substantially in the opening; and a second electrode formed on the light emitting member and the auxiliary electrode.

[0012] The organic light emitting display may further include: a gate line transmitting gate signals; a data line transmitting data signals; a switching transistor connected to the gate line and the data line; a signal transmission line transmitting driving signals; and a driving transistor connected to the signal transmission line and the first electrode and controlled by the data signals;

[0013] The switching transistor and the driving transistor may be connected to each other and the organic light emitting display further comprising a storage capacitor connected between the switching transistor and the signal transmission line.

[0014] The first electrode may include reflective material, and the second electrode may include transparent material.

[0015] The auxiliary electrode preferably has a resistivity lower than the second electrode.

[0016] An organic light emitting display is provided, which includes: first and second semiconductor members including first and second intrinsic portions, respectively, and including amorphous silicon or polysilicon; a plurality of gate conductors that include a gate line including a first gate electrode overlapping the first intrinsic portion and a second gate electrode overlapping the second intrinsic portion; a gate insulating layer disposed between the first and the second semiconductor members and the gate conductors; a plurality of data conductors that includes a data line including a first source electrode connected to the first semiconductor member, a first drain electrode opposing the first source electrode with respect to the first intrinsic portion and connected to the first semiconductor member, a voltage transmission line including a second source electrode connected to the second semiconductor member, and a second drain electrode opposing the second source electrode with respect to the second intrinsic portion and connected to the second semiconductor member; a pixel electrode connected to the second drain electrode; a partition having an opening exposing the pixel electrode at least in part; an auxiliary electrode formed on the partition and having substantially the same planar shape as the partition; an organic light emitting member formed on the pixel electrode and disposed substantially in the opening; and a common electrode formed on the light emitting member and the auxiliary electrode.

[0017] The pixel electrode may include reflective material and the common electrode may include transparent material.

[0018] The auxiliary electrode preferably has a resistivity lower than the common electrode.

[0019] The organic light emitting display may further include a connecting member connecting the first drain electrode and the second gate electrode.

[0020] A method of manufacturing an organic light emitting display is provided, which includes: forming a plurality of first display electrodes; forming a partition having a plurality of openings exposing the first display electrodes at least in part; forming an auxiliary electrode on the partition; forming a plurality of organic light emitting members in the openings; and forming a second display electrode on the light emitting member and the auxiliary electrode, wherein the formation of the partition and the formation of the auxiliary electrode are performed by using a single lithography.

[0021] The formation of the partition and the formation of the auxiliary electrode may include: sequentially depositing an insulating layer and a conductively layer; forming a first photoresist on the conductive layer; sequentially etching the conductive layer and the insulating layer using the first photoresist as an etch mask to form a conductor and the partition; ashing the first photoresist to form a second photoresist; and etching the conductor to form the auxiliary electrode using the second photoresist as an etch mask.

[0022] The first display electrodes may include reflective material and the second display electrode may include transparent material.

[0023] A method of manufacturing an organic light emitting display is provided, which includes: forming first and second semiconductor members including amorphous silicon or polysilicon; forming a gate line including a first gate electrode and a second gate electrode; forming a gate insulating layer between the first and the second semiconductor members and the gate line and the second gate electrode; forming a data line including a first source electrode, a voltage transmission line, and first and second drain electrodes; forming a passivation layer on the data line, the voltage transmission line, and the first and the second drain electrodes; forming a pixel electrode on the passivation layer, the pixel electrode connected to the second drain electrode; forming a partition having an opening exposing the pixel electrode at least in part; forming an auxiliary electrode on the partition; forming an organic light emitting member in the opening; and forming a common electrode on the light emitting member and the auxiliary electrode.

[0024] The formation of the partition and the formation of the auxiliary electrode may include: sequentially depositing an insulating layer and a conductively layer; forming a first photoresist on the conductive layer; sequentially etching the conductive layer and the insulating layer using the first photoresist as an etch mask to form a conductor and the partition; ashing the first photoresist to form a second photoresist; and etching the conductor to form the auxiliary electrode using the second photoresist as an etch mask.

[0025] The pixel electrode may include reflective material and the common electrode may include transparent material.

[0026] The auxiliary electrode may have a resistivity lower than the common electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The present invention will become more apparent by describing preferred embodiments thereof in detail with reference to the accompanying drawings in which:

[0028] **FIG. 1** is a layout view of an OLED according to an embodiment of the present invention;

[0029] **FIGS. 2 and 3** are sectional views of the OLED shown in **FIG. 1** taken along the lines II-II' and III-III', respectively;

[0030] **FIGS. 11, 13, 15, 17, 19, 21** and **23** are layout views of the OLED shown in **FIGS. 1-3** in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention;

[0031] **FIGS. 4, 6, 8, 10, 12, 14, 16** and **18** are layout views of the OLED shown in **FIGS. 1-3** in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention;

[0032] **FIGS. 5A and 5B** are sectional views of the OLED shown in **FIG. 4** taken along the lines VA-VA' and VB-VB', respectively;

[0033] **FIGS. 7A and 7B** are sectional views of the OLED shown in **FIG. 6** taken along the lines VIIA-VIIA' and VIIB-VIIB', respectively;

[0034] **FIGS. 9A and 9B** are sectional views of the OLED shown in **FIG. 8** taken along the lines IXA-IXA' and IXB-IXB', respectively;

[0035] **FIGS. 11A and 11B** are sectional views of the OLED shown in **FIG. 10** taken along the lines XIA-XIA' and XIB-XIB', respectively;

[0036] **FIGS. 13A and 13B** are sectional views of the OLED shown in **FIG. 12** taken along the lines XIIIA-XIIIA' and XIIIB-XIIIB', respectively;

[0037] **FIGS. 15A and 15B** are sectional views of the OLED shown in **FIG. 14** taken along the lines XVA-XVA' and XVB-XVB', respectively;

[0038] **FIGS. 17A and 17B** are sectional views of the OLED shown in **FIG. 16** taken along the lines XVIIA-XVIIA' and XVIIB-XVIIB', respectively;

[0039] **FIGS. 19A and 19B** are sectional views of the OLED shown in **FIG. 18** taken along the lines XIXA-XIXA' and XIXB-XIXB', respectively;

[0040] **FIGS. 20A and 20B** are sectional views of the OLED shown in **FIG. 18** taken along the lines XIXA-XIXA' and XIXB-XIXB', respectively, and illustrate the first step of forming the structure shown in **FIGS. 19A and 19B;**

[0041] **FIGS. 21A and 21B** are sectional views of the OLED shown in **FIG. 18** taken along the lines XIXA-XIXA' and XIXB-XIXB', respectively, and illustrate the step following the step shown in **FIGS. 20A and 20B**;

[**0042**] and **FIGS. 22A and 22B** are sectional views of the OLED shown in **FIG. 18** taken along the lines XIXA-XIXA' and XIXB-XIXB', respectively, and illustrate the step following the step shown in **FIGS. 21A and 21B**;

[**0043**] **FIG. 23** is a layout view of an OLED according to another embodiment of the present invention;

[**0044**] **FIGS. 24 and 25** are sectional views of the OLED taken along the lines XXIV-XXIV' and XXV-XXV';

[**0045**] **FIGS. 26, 28, 30, 32, 34** and **36** are layout views of the OLED shown in **FIGS. 23-25** in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention;

[**0046**] **FIGS. 27A and 27B** are sectional views of the OLED shown in **FIG. 26** taken along the lines XXVIIA-VA' and XXVIIB-XXVIIB', respectively;

[**0047**] **FIGS. 29A and 29B** are sectional views of the OLED shown in **FIG. 28** taken along the lines XXIXA-XXIXA' and XXIXB-XXIXB', respectively;

[**0048**] **FIGS. 31A and 31B** are sectional views of the OLED shown in **FIG. 30** taken along the lines XXXIA-XXXIA' and XXXIB-XXXIB', respectively;

[**0049**] **FIGS. 33A and 33B** are sectional views of the OLED shown in **FIG. 32** taken along the lines XXXIIIA-XXXIIIA' and XXXIIIB-XXXIIIB', respectively;

[**0050**] **FIGS. 35A and 35B** are sectional views of the OLED shown in **FIG. 34** taken along the lines XXXVA-XXXVA' and XXXVB-XXXVB', respectively; and

[**0051**] **FIGS. 37A and 37B** are sectional views of the OLED shown in **FIG. 36** taken along the lines XXXVIIA-XXXVIIA' and XXXVIIB-XXXVIIB', respectively.

DETAILED DESCRIPTION OF EMBODIMENTS

[**0052**] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

[**0053**] In the drawings, the thickness of layers, films, panels, regions, etc. are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[**0054**] Now, OLEDs and manufacturing methods thereof according to embodiments of the present invention will be described with reference to accompanying drawings.

[**0055**] Now, an OLED according to an embodiment of the present invention is described in detail with reference to **FIGS. 1-3**.

[**0056**] **FIG. 1** is a layout view of an OLED according to an embodiment of the present invention, **FIGS. 2 and 3** are sectional views of the OLED shown in **FIG. 1** taken along the lines II-II' and III-III', respectively.

[**0057**] A blocking layer **111** preferably made of silicon oxide or silicon nitride is formed on an insulating substrate **110** preferably made of transparent glass. The blocking film **111** may have a dual-layered structure.

[**0058**] A plurality of semiconductor islands **151***a* and **151***b* preferably made of polysilicon are formed on the blocking film **111**. Each of the semiconductor islands **151***a* and **151***b* includes a plurality of extrinsic regions containing N type or P type conductive impurity and at least one intrinsic region hardly containing conductive impurity.

[**0059**] Regarding a semiconductor island **151***a* for a switching TFT Qa, the extrinsic regions include a first source region **153***a*, an intermediate region **1535**, and a first drain region **155***a*, which are doped with N type impurity and separated from one another, and the intrinsic regions include such as a pair of (first) channel regions **154***a***1** and **154***a***2** disposed between the extrinsic regions **153***a*, **1535** and **155***a*.

[**0060**] Concerning a semiconductor island **151***b* for a driving TFT Qb, the extrinsic regions include a second source region **153***b* and a second drain region **155***b*, which are doped with P type impurity and separated from one another, and the intrinsic region includes a channel region **154***b* disposed between the second source region **153***b* and the second drain region **155***b*. The second source region **153***b* extends to form a storage region **157**.

[**0061**] The extrinsic regions may further include lightly doped regions (not shown) disposed between the channel regions **154***a***1**, **154***a***2** and **154***b* and the source and the drain regions **153***a*, **155***a*, **153***b* and **155***b*. The lightly doped regions may be substituted with offset regions that contain substantially no impurity.

[**0062**] Alternatively, the extrinsic regions **153***a* and **155***a* of the first semiconductor islands **151***a* are doped with P type impurity, while the extrinsic regions **153***b* and **155***b* of the second semiconductor islands **151***b* are doped with N type impurity, depending on driving conditions. The conductive impurity includes P type impurity such as boron (B) and gallium (Ga) and N type impurity such as phosphorous (P) and arsenic (As).

[**0063**] A gate insulating layer **140** preferably made of silicon oxide or silicon nitride is formed on the semiconductor islands **151***a* and **151***b* and the blocking film **111**.

[**0064**] A plurality of gate conductors including a plurality of gate lines **121** including a plurality of pairs of first gate electrodes **124***a* and a plurality of second gate electrodes **124***b* are formed on the gate insulating layer **140**.

[**0065**] The gate lines **121** for transmitting gate signals extend substantially in a transverse direction. Each pair of first gate electrodes **124***a* protrude upward from the gate line **121** and they intersect the first semiconductor islands **151***a* such that they overlap the pair of the first channel regions **154***a*. Each gate line **121** may include an expanded end portion having a large area for contact with another layer or an external driving circuit. The gate lines **121** may be directly connected to a gate driving circuit for generating the gate signals, which may be integrated on the substrate **110**.

[**0066**] The second gate electrodes **124***b* are separated from the gate lines **121** and intersect the second semiconductor islands **151***b* such that they overlap the second channel regions **154***b*. The second gate electrodes **124***b* extend to form storage electrodes **127** overlapping the storage electrode regions **157** of the second semiconductor islands **151***b* to form storage capacitors Cst.

[**0067**] The gate conductors **121** and **124***b* are preferably made of low resistivity material including Al containing metal such as Al and Al alloy (e.g. Al—Nd), Ag containing metal such as Ag and Ag alloy, and Cu containing metal such as Cu and Cu alloy. The gate conductors **121** and **124***b* may have a multi-layered structure including two films having different physical characteristics. One of the two films is preferably made of low resistivity metal including Al containing metal, Ag containing metal, and Cu containing metal for reducing signal delay or voltage drop in the gate conductors **121** and **124***b*. The other film is preferably made of material such as Cr, Mo and Mo alloy, Ta or Ti, which has good physical, chemical, and electrical contact characteristics with other materials such as indium tin oxide (ITO) or indium zinc oxide (IZO). Good examples of the combination of the two films are a lower Cr film and an upper Al—Nd alloy film and a lower Al film and an upper Mo film.

[**0068**] In addition, the lateral sides of the gate conductors **121** and **124***b* are inclined relative to a surface of the substrate **110**, and the inclination angle thereof ranges about 30-80 degrees.

[**0069**] An interlayer insulating film **160** is formed on the gate conductors **121** and **124***b*. The interlayer insulating layer **160** is preferably made of photosensitive organic material having a good flatness characteristic, low dielectric insulating material such as a-Si:C:O and a-Si:O:F formed by plasma enhanced chemical vapor deposition (PECVD), or inorganic material such as silicon nitride and silicon oxide.

[**0070**] The interlayer insulating layer **160** has a plurality of contact holes **164** exposing the second gate electrodes **124***b*. In addition, the interlayer insulating layer **160** and the gate insulating layer **140** have a plurality of contact holes **163***a*, **163***b*, **165***a* and **165***b* exposing the source regions **153***a* and **153***b* and the drain regions **155***a* and **155***b*, respectively.

[**0071**] A plurality of data conductors including a plurality of data lines **171**, a plurality of voltage transmission lines **172**, and a plurality of first and second drain electrodes **175***a* and **175***b* are formed on the interlayer insulating film **160**.

[**0072**] The data lines **171** for transmitting data signals extend substantially in the longitudinal direction and intersect the gate lines **121**. Each data line **171** includes a plurality of first source electrodes **173***a* connected to the first source regions **153***a* through the contact holes **163***a*. Each data line **171** may include an expanded end portion having a large area for contact with another layer or an external driving circuit. The data lines **171** may be directly connected to a data driving circuit for generating the gate signals, which may be integrated on the substrate **110**.

[**0073**] The voltage transmission lines **172** for transmitting driving voltages for the driving TFT Qb extend substantially in the longitudinal direction and intersect the gate lines **121**. Each voltage transmission line **172** includes a plurality of second source electrodes **173***b* connected to the second source regions **153***b* through the contact holes **163***b*. The voltage transmission lines **171** may be connected to each other.

[**0074**] The first drain electrodes **175***a* are separated from the data lines **171** and the voltage transmission lines **172** and connected to the first drain regions **155***a* through the contact holes **165** and to the second gate electrodes **124***b* through the contact hole **164**.

[**0075**] The second drain electrodes **175***b* are separated from the data lines **171** and the voltage transmission lines **172** and connected to the second drain regions **155***b* through the contact holes **165***b*.

[**0076**] The data conductors **171**, **172**, **175***a* and **175***b* are preferably made of refractory metal including Cr, Mo, Ti, Ta or alloys thereof. They may have a multi-layered structure preferably including a low resistivity film and a good contact film. A good example of the multi-layered structure includes a Mo lower film, an Al middle film, and a Mo upper film as well as the above-described combinations of a Cr lower film and an Al—Nd upper film and an Al lower film and a Mo upper film.

[**0077**] Like the gate conductors **121** and **124***b*, the data conductors **171**, **172**, **175***a* and **175***b* have tapered lateral sides relative to the surface of the substrate **110**, and the inclination angles thereof range about 30-80 degrees.

[**0078**] A passivation layer **180** is formed on the data conductors **171**, **172**, **175***a* and **175***b*. The passivation layer **180** is also preferably made of photosensitive organic material having a good flatness characteristic, low dielectric insulating material such as a-Si:C:O and a-Si:O:F formed by PECVD, or inorganic material such as silicon nitride and silicon oxide.

[**0079**] The passivation layer **180** has a plurality of contact holes **185** exposing the second drain electrodes **175***b*. The passivation layer **180** may further has a plurality of contact holes (not shown) exposing end portions of the data lines **171** and the passivation layer **180** and the interlayer insulating layer **160** may have a plurality of contact holes (not shown) exposing end portions of the gate lines **121**.

[**0080**] A plurality of pixel electrodes **190** are formed on the passivation layer **180**. The pixel electrodes **190** are connected to the second drain electrodes **175***b* through the contact holes **185** and they are preferably made of at least one of reflective opaque material such as Al or Ag alloy. However, the pixel electrode **190** may be made of transparent conductor such as ITO or IZO and opaque reflective conductor such as Al, Ag, Ca, Ba and Mg. The pixel electrode **190** may be incorporated with the second drain electrode **175***b* for reducing the manufacturing cost.

[**0081**] A plurality of contact assistants or connecting members (not shown) may be also formed on the passivation layer **180** such that they are connected to the exposed end portions of the gate lines **121** or the data lines **171**.

[**0082**] A partition **32** for separating pixels of the OLED is formed on the passivation layer **180** and the pixel electrodes **190**. The partition **32** surrounds the pixel electrodes **190** like a bank to define openings to be filled with organic light emitting material. The partition **32** is preferably made of organic or inorganic insulating material.

[**0083**] A plurality of light emitting members **30** are formed on the pixel electrodes **190** and disposed in the openings defined by the partition **32**. The light emitting members **30** are preferably made of organic material emitting primary-color lights such as red, green and blue lights. The red, green and blue light emitting members **30** are periodically arranged.

[**0084**] An auxiliary electrode **272** preferably made of low resistivity material such as metal is formed on the partition **32**. The auxiliary electrode **272** has substantially the same planar shape as the partition **32**.

[**0085**] A common electrode **270** supplied with a predetermined voltage such as a common voltage is formed on the light emitting members **30**, the auxiliary electrode **272**, and the partition **32**. The common electrode **270** is preferably made of transparent conductive material such as ITO and IZO or opaque metal such as Al, Ag, Ca, Ba and Mg. The common electrode **270** contacts the auxiliary electrode **272** such that the auxiliary electrode **272** compensates the conductivity of the common electrode **270** and prevents the distortion of the signals transmitted to the common electrode **270**.

[**0086**] In the above-described OLED, a first semiconductor island **151***a*, a first gate electrode **124***a* connected to the gate line **121**, a first source electrode **153***a* connected to the data line **171**, and a first drain electrode **155***a* form a switching TFT Qa. In addition, a second semiconductor island **151***b*, a second gate electrode **124***b* connected to the first drain electrode **155***a*, a second source electrode **153***b* connected to the voltage transmission line **172**, and a second drain electrode **155***b* connected to a pixel electrode **190** form a driving TFT Qb. Furthermore, a pixel electrode **190** and a common electrode **270** serve as an anode and a cathode, respectively, and a storage region **157** connected to a first drain region **155***a* and a storage electrode **127** connected to a voltage transmission line **172** through a second source electrode **153***b* form a storage capacitor Cst. The TFTs Qa and Qb shown in **FIGS. 1-3** are referred to as "top gate TFTs" since the gate electrodes **124***a* and **124***b* are disposed on the semiconductors **151***a* and **151***b*.

[**0087**] The switching TFT Qa transmits data signals from the data line **171** to the driving TFT Qb in response to the gate signal from the gate line **121**. Upon the receipt of the data signal, the driving TFT Qb generates a current having a magnitude depending on the voltage difference between the second gate electrode **124***b* and the second source electrode **173***b*. In addition, the voltage difference is charged in the storage capacitor Cst to be maintained after the switching TFT Qa is turned off. The current driven by the driving TFT Qb enters into the light emitting member **30** through the pixel electrode **190** and reaches the common electrode **270**. The current flowing in the light emitting member **30** means that positive charge carriers such as holes and negative charge carriers such as electrons are injected into the light emitting member **30** from the anode **190** and the cathode **270**, respectively, and they are drifted by an electric field generated by the voltage difference between the anode **190** and the cathode **270**. The holes and the electrons in the light emitting member **30** then meet each other to be recombined into excitons, which emit light with a predetermined wavelength. The intensity of the emitted light depends on the current driven by the driving TFT Qb and flowing in the light emitting member **30**.

[**0088**] The emitted light goes out of the display panel after passing through the common electrode **270** or the pixel electrode **190**. A transparent common electrode **270** and an opaque pixel electrode **190** are applicable to a top emission type OLED, which displays an image on its top surface. On the contrary, a transparent pixel electrode **190** and an opaque common electrode **270** are applicable to a bottom emission type OLED, which displays an image on its bottom surface.

[**0089**] Now, a method of manufacturing the OLED shown in **FIGS. 1-3** is described with reference to **FIGS. 11-24B** as well as **FIGS. 1-3**.

[**0090**] **FIGS. 4, 6, 8, 10, 12, 14, 16** and **18** are layout views of the OLED shown in **FIGS. 1-3** in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention, **FIGS. 5A and 5B** are sectional views of the OLED shown in **FIG. 4** taken along the lines VA-VA' and VB-VB', respectively, **FIGS. 7A and 7B** are sectional views of the OLED shown in **FIG. 6** taken along the lines VIIA-VIIA' and VIIB-VIIB', respectively, **FIGS. 9A and 9B** are sectional views of the OLED shown in **FIG. 8** taken along the lines IXA-IXA' and IXB-IXB', respectively, **FIGS. 11A and 11B** are sectional views of the OLED shown in **FIG. 10** taken along the lines XIA-XIA' and XIB-XIB', respectively, **FIGS. 13A and 13B** are sectional views of the OLED shown in **FIG. 12** taken along the lines XIIIA-XIIIA' and XIIIB-XIIIB', respectively, **FIGS. 15A and 15B** are sectional views of the OLED shown in **FIG. 14** taken along the lines XVA-XVA' and XVB-XVB', respectively, **FIGS. 17A and 17B** are sectional views of the OLED shown in **FIG. 16** taken along the lines XVIIA-XVIIA' and XVIIB-XVIIB', respectively, **FIGS. 19A and 19B** are sectional views of the OLED shown in **FIG. 18** taken along the lines XIXA-XIXA' and XIXB-XIXB', respectively, **FIGS. 20A and 20B** are sectional views of the OLED shown in **FIG. 18** taken along the lines XIXA-XIXA' and XIXB-XIXB', respectively, and illustrate the first step of forming the structure shown in **FIGS. 19A and 19B; FIGS. 21A and 21B** are sectional views of the OLED shown in **FIG. 18** taken along the lines XIXA-XIXA' and XIXB-XIXB', respectively, and illustrate the step following the step shown in **FIGS. 20A and 20B**; and **FIGS. 22A and 22B** are sectional views of the OLED shown in **FIG. 18** taken along the lines XIXA-XIXA' and XIXB-XIXB', respectively, and illustrate the step following the step shown in **FIGS. 21A and 21B**.

[**0091**] A blocking layer **111** is formed on an insulating substrate **110**, and a semiconductor layer made of amorphous silicon is deposited on the blocking layer **111** preferably by LPCVD (low temperature chemical vapor deposition), PECVD (plasma enhanced chemical vapor deposition) or sputtering.

[**0092**] Next, the semiconductor layer is crystallized into polysilicon and photo-etched to form a plurality of pairs of first and second semiconductor islands **151***a* and **151***b* as shown in **FIGS. 4-5B**.

[**0093**] Referring to **FIGS. 6-7B**, a gate insulating layer **140** and a gate metal layer are sequentially deposited on the gate insulating layer **140** and a first photoresist PR1 is formed thereon. The gate metal layer is etched by using the first photoresist PR1 as an etch mask to form a plurality of gate electrodes **124***b* including storage electrodes **127** and a plurality of gate metal members **120***a*. P type impurity is introduced into portions of the second semiconductor islands **151***b*, which are not covered with the gate electrodes **124***b* and the gate metal members **120***a* as well as the first photoresist PR1, to form a plurality of P type extrinsic regions **153***b* and **155***b*. At this time, the first semiconductor islands **151***a* are covered with the first photoresist PR1 and the gate metal members **120***a* to be protected from impurity implantation.

[0094] Referring to **FIGS. 8-9B**, the first photoresist PR1 is removed and a second photoresist PR2 is formed. The gate metal members **120***a* is etched by using the second photoresist PR2 as an etch mask to form a plurality of gate lines **121** including gate electrodes **124***a*. N type impurity is injected into portions of the first semiconductor islands **151***a*, which are not covered with the gate lines **121** and the gate electrodes **124***b* as well as the second photoresist PR2, to form a plurality of N type extrinsic regions **153***a* and **155***a*. At this time, the second semiconductor islands **151***b* are covered with the second photoresist PR2 to be protected from impurity implantation.

[0095] Referring to **FIGS. 10-11B**, an interlayer insulating film **160** is deposited and the interlayer insulating film **160** and the gate insulating layer **140** are photo-etched form a plurality of contact holes **163***a*, **163***b*, **165***a* and **165***b* exposing the extrinsic regions **153***a*, **155***a*, **153***b* and **155***b*, respectively, as well as a plurality of contact holes **164** exposing the gate electrodes **124***b*.

[0096] Referring to **FIGS. 12-13B**, a plurality of data conductors including a plurality of data lines **171** including first source electrodes **173***a*, a plurality of voltage transmission line **172**, a plurality of first and second drain electrodes **175***a* and **175***b* are formed on the interlayer insulating layer **160**.

[0097] Referring to **FIGS. 14-15B**, a passivation layer **180** is deposited and is photo-etched to form a plurality of contact holes **185** exposing the second drain electrodes **175***b*.

[0098] Referring to **FIGS. 16-17B**, a plurality of pixel electrodes **190** are formed on the passivation layer **180**. When the pixel electrodes **190** are made of reflective opaque material, they may be formed of the data metal layer along with the data lines **171**.

[0099] Referring to **FIGS. 18-19B**, an insulating layer and a conductive layer are sequentially deposited and patterned to form a partition **32** and an auxiliary electrode **272**, respectively, using a single photolithography such that the partition **32** and the auxiliary electrode **272** have substantially the same planar shape, which will be described in detail with reference to **FIGS. 20A-22B**.

[0100] Referring to **FIGS. 20A and 20B**, an insulating layer and a conductive layer are sequentially deposited and a third photoresist PR3 is formed on the conductive layer. The conductive layer is etched by using the third photoresist PR3 as an etch mask to form a pre-electrode **272**' and the insulating layer is etched to form a partition **32**. The etch of the conductive layer and the insulating layer generates undercut such that edges of the pre-electrode **272**' are located under the third photoresist PR3 and edges of the partition **32** are located under the pre-electrode **272**'.

[0101] Referring to **FIGS. 21A and 21B**, the third photoresist PR3 is subjected to ashing to form a fourth photoresist PR4 having edges disposed on the pre-electrode **272**' such that edge portions of the pre-electrode **272**' are exposed.

[0102] Referring to **FIGS. 22A and 22B**, the pre-electrode **272**' is etched by using the fourth photoresist PR4 as an etch mask to form an auxiliary electrode **272**. The etch also generates undercut such that edges of the auxiliary electrode **272** lies under the fourth photoresist PR4 and on the partition **32**.

[0103] Finally, the fourth photoresist PR4 is removed as shown in **FIGS. 19A and 19B**.

[0104] The formation of the partition **32** and the auxiliary electrode **272** with a single photolithography step simplifies the manufacturing process and thus reduces the manufacturing cost. In addition, this process facilitates to manufacture a large OLED.

[0105] Referring to **FIGS. 1-3**, a plurality of organic light emitting members **30** preferably including multiple layers are formed in the openings by deposition or ink-jet printing following a masking, and a common electrode **270** are subsequently formed.

[0106] A buffer layer (not shown) preferably made of conductive organic material may be formed before the formation of the common electrode **270**.

[0107] Now, an OLED having bottom gate TFTs according to an embodiment of the present invention will be described in detail with reference to **FIGS. 23-25**.

[0108] **FIG. 23** is a layout view of an OLED according to another embodiment of the present invention and **FIGS. 24 and 25** are sectional views of the OLED taken along the lines XXIV-XXIV' and XXV-XXV'.

[0109] A plurality of gate conductors that include a plurality of gate lines **121** including first gate electrodes **124***a* and a plurality of second gate electrodes **124***b* are formed on an insulating substrate **110** such as transparent glass.

[0110] The gate lines **121** transmitting gate signals extend substantially in a transverse direction and are separated from each other. The first gate electrodes **124***a* protrude upward. The gate lines **121** may extend to be connected to a driving circuit (not shown) integrated on the substrate **110**, or it may have an end portion (not shown) having a large area for connection with another layer or an external driving circuit mounted on the substrate **110** or on another device such as a flexible printed circuit film (not shown) that may be attached to the substrate **110**.

[0111] Each of the second gate electrodes **124***b* are separated from the gate lines **121** and includes a storage electrode **127** extending substantially in a transverse direction between two adjacent gate lines **121**.

[0112] The gate conductors **121** and **124***b* are preferably made of Al containing metal such as Al and Al alloy, Ag containing metal such as Ag and Ag alloy, Cu containing metal such as Cu and Cu alloy, Mo containing metal such as Mo and Mo alloy, Cr, Ti or Ta. The gate conductors **121** and **124***b* may have a multi-layered structure including two films having different physical characteristics. One of the two films is preferably made of low resistivity metal including Al containing metal, Ag containing metal, or Cu containing metal for reducing signal delay or voltage drop in the gate conductors **121** and **124***b*. On the other hand, the other film is preferably made of material such as Cr, Mo, Mo alloy, Ta, or Ti, which has good physical, chemical, and electrical contact characteristics with other materials such as indium tin oxide (ITO) or indium zinc oxide (IZO). Good examples of the combination of the two films are a lower Cr film and an upper Al—Nd alloy film and a lower Al film and an upper Mo film.

[0113] In addition, the lateral sides of the gate conductors **121** and **124*b*** are inclined relative to a surface of the substrate **110**, and the inclination angle thereof ranges about 30-80 degrees.

[0114] A gate insulating layer **140** preferably made of silicon nitride (SiNx) is formed on the gate conductors **121** and **124*b***.

[0115] A plurality of semiconductor stripes and islands **151** and **154*b*** preferably made of hydrogenated amorphous silicon (abbreviated to "a-Si") or polysilicon are formed on the gate insulating layer **140**. Each semiconductor stripe **151** extends substantially in the longitudinal direction and has a plurality of projections **154*a*** branched out toward the first gate electrodes **124*a***. Each semiconductor island **154*b*** crosses a second gate electrode **124*b*** and includes a portion overlapping the storage electrode **127** of the second gate electrode **124*b***.

[0116] A plurality of ohmic contact stripes **161** and ohmic contact islands **163*b***, **165*a*** and **165*b***, which are preferably made of silicide or n+hydrogenated a-Si heavily doped with n type impurity such as phosphorous, are formed on the semiconductor stripes and islands **151** and **154*b***. Each ohmic contact stripe **161** has a plurality of projections **163*a***, and the projections **163*a*** and the ohmic contact islands **165*a*** are located in pairs on the projections **154*a*** of the semiconductor stripes **151**. The ohmic contact islands **163*b*** and **165*b*** are located in pairs on the semiconductor islands **154*b***.

[0117] The lateral sides of the semiconductor stripes and islands **151** and **154*b*** and the ohmic contacts **161**, **163*b***, **165*b*** and **165*b*** are inclined relative to a surface of the substrate, and the inclination angles thereof are preferably in a range between about 30-80 degrees.

[0118] A plurality of data conductors including a plurality of data lines **171**, a plurality of voltage transmission lines **172**, and a plurality of first and second drain electrodes **175*a*** and **175*b*** are formed on the ohmic contacts **161**, **163*b***, **165*b*** and **165*b*** and the gate insulating layer **140**.

[0119] The data lines **171** for transmitting data signals extend substantially in the longitudinal direction and intersect the gate lines **121**. Each data line **171** includes a plurality of first source electrodes **173*a*** an end portion having a large area for contact with another layer or an external device. The data lines **171** may be directly connected to a data driving circuit for generating the gate signals, which may be integrated on the substrate **110**.

[0120] The voltage transmission lines **172** for transmitting driving voltages extend substantially in the longitudinal direction and intersect the gate lines **121**. Each voltage transmission line **172** includes a plurality of second source electrodes **173*b***. The voltage transmission lines **171** may be connected to each other.

[0121] The first and the second drain electrodes **175*a*** and **175*b*** are separated from the data lines **171** and the voltage transmission lines **172** and from each other. Each pair of the first source electrodes **173*a*** and the first drain electrodes **175*a*** are disposed opposite each other with respect to a first gate electrode **124*a***, and each pair of the second source electrodes **173*b*** and the second drain electrodes **175*b*** are disposed opposite each other with respect to a second gate electrode **124*b***.

[0122] A first gate electrode **124*a***, a first source electrode **173*a***, and a first drain electrode **175*a*** along with a projection **154*a*** of a semiconductor stripe **151** form a switching TFT Qa having a channel formed in the projection **154*a*** disposed between the first source electrode **173*a*** and the first drain electrode **175*a***. Meanwhile, a second gate electrode **124*b***, a second source electrode **173*b***, and a second drain electrode **175*b*** along with a semiconductor island **154*b*** form a driving TFT Qb having a channel formed in the semiconductor island **154*b*** disposed between the second source electrode **173*b*** and the second drain electrode **175*b***.

[0123] The data conductors **171**, **172**, **175*a*** and **175*b*** are preferably made of refractory metal including Cr, Mo, Ti, Ta or alloys thereof. They may have a multi-layered structure preferably including a low resistivity film and a good contact film. A good example of the multi-layered structure includes a Mo lower film, an Al middle film, and a Mo upper film as well as the above-described combinations of a Cr lower film and an Al—Nd upper film and an Al lower film and a Mo upper film.

[0124] Like the gate conductors **121** and **124*b***, the data conductors **171**, **172**, **175*a*** and **175*b*** have tapered lateral sides relative to the surface of the substrate **110**, and the inclination angles thereof range about 30-80 degrees.

[0125] The ohmic contacts **161**, **163*b***, **165*b*** and **165*b*** are interposed only between the underlying semiconductor stripes and islands **151** and **154*b*** and the overlying data conductors **171**, **172**, **175*a*** and **175*b*** thereon and reduce the contact resistance therebetween. The semiconductor stripes **151** include a plurality of exposed portions, which are not covered with the data conductors **171**, **172**, **175*a*** and **175*b***.

[0126] A passivation layer **180** is formed on the data conductors **171**, **172**, **175*a*** and **175*b*** and the exposed portions of the semiconductor stripes and islands **151** and **154*b***. The passivation layer **180** is preferably made of inorganic material such as silicon nitride or silicon oxide, photosensitive organic material having a good flatness characteristic, or low dielectric insulating material having dielectric constant lower than 4.0 such as a-Si:C:O and a-Si:O:F formed by plasma enhanced chemical vapor deposition (PECVD). The passivation layer **180** may include a lower film of inorganic insulator and an upper film of organic insulator.

[0127] The passivation layer **180** has a plurality of contact holes **184**, **185*a*** and **185*b*** exposing portions of the second gate electrodes **124*b*** and the first and the second drain electrodes **175*a*** and **175*b***, respectively.

[0128] A plurality of pixel electrodes **190** and a plurality of connecting members **85** are formed on the passivation layer **180**. The pixel electrodes **190** are connected to the second drain electrodes **175*b*** through the contact holes **185*b*** and they are preferably made of at least one of reflective opaque material such as Al or Ag alloy. However, the pixel electrode **190** may be made of transparent conductor such as ITO or IZO and opaque reflective conductor such as Al, Ag, Ca, Ba and Mg. The pixel electrode **190** may be incorporated with the second drain electrode **175***b* for reducing the manufacturing cost.

[0129] A plurality of contact assistants or connecting members (not shown) may be also formed on the passivation layer **180** such that they are connected to the exposed end portions of the gate lines **121** or the data lines **171**.

[0130] A partition **32**, an auxiliary electrode **272**, a plurality of light emitting members **30**, and a common electrode **270** are formed on the passivation layer **180**, the pixel electrodes **190**, and the connecting members **85** like those shown in **FIGS. 1-3**.

[0131] A method of manufacturing the TFT array panel shown in **FIGS. 23-25** according to an embodiment of the present invention will be now described in detail with reference to FIGS. **26** to 37B as well as **FIGS. 23-25**.

[0132] **FIGS. 26, 28, 30, 32, 34** and **36** are layout views of the OLED shown in **FIGS. 23-25** in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention, **FIGS. 27A and 27B** are sectional views of the OLED shown in **FIG. 26** taken along the lines XXVIIA-VA' and XXVIIB-XXVIIB', respectively, **FIGS. 29A and 29B** are sectional views of the OLED shown in **FIG. 28** taken along the lines XXIXA-XXIXA' and XXIXB-XXIXB', respectively, **FIGS. 31A and 31B** are sectional views of the OLED shown in **FIG. 30** taken along the lines XXXIA-XXXIA' and XXXIB-XXXIB', respectively, **FIGS. 33A and 33B** are sectional views of the OLED shown in **FIG. 32** taken along the lines XXXIIIA-XXXIIIA' and XXXIIIB-XXXIIIB', respectively, **FIGS. 35A and 35B** are sectional views of the OLED shown in **FIG. 34** taken along the lines XXXVA-XXXVA' and XXXVB-XXXVB', respectively, and **FIGS. 37A and 37B** are sectional views of the OLED shown in **FIG. 36** taken along the lines XXXVIIA-XXXVIIA' and XXXVIIB-XXXVIIB', respectively.

[0133] Referring to **FIGS. 26-27B**, a plurality of gate conductors that includes a plurality of gate lines **121** including first gate electrodes **124***a* and a plurality of second gate electrodes **124***b* including storage electrodes **127** are formed on a substrate such as transparent glass.

[0134] Referring to **FIGS. 28-29B**, after sequential deposition of a gate insulating layer **140**, an intrinsic a-Si layer, and an extrinsic a-Si layer, the extrinsic a-Si layer and the intrinsic a-Si layer are photo-etched to form a plurality of extrinsic semiconductor stripes and islands **164***a* and **164***b* and a plurality of intrinsic semiconductor stripes and islands **151** and **154***b* including projections **154***a* on the gate insulating layer **140**. The gate insulating layer **140** is preferably made of silicon nitride with thickness of about 2,000 Å to about 5,000 Å, and the deposition temperature is preferably in a range of about 250-500° C.

[0135] Referring to **FIGS. 30-31B**, a conductive layer is sputtered and etched using a photoresist (not shown) to form a plurality of data conductors that includes a plurality of data lines **171** including first source electrodes **173***a*, a plurality of voltage transmission lines **172** including second source electrodes **173***b*, and a plurality of first and second drain electrodes **175***a* and **175***b*.

[0136] Before or after removing the photoresist, portions of the extrinsic semiconductor stripes **164**, which are not covered with the data conductors **171, 172, 175***a* and **175***b*, are removed by etch to complete a plurality of ohmic contact stripes **161** including projections **163***a* and a plurality of ohmic contact islands **163***b*, **165***a* and **165***b* and to expose portions of the intrinsic semiconductor stripes and islands **151** and **154***b*.

[0137] Oxygen plasma treatment may follow thereafter in order to stabilize the exposed surfaces of the semiconductor stripes **151**.

[0138] Referring to **FIGS. 32-33B**, a passivation layer **180** is deposited and patterned to form a plurality of contact holes **184**, **185***a* and **185***b* exposing the first gate electrodes **124***b* and the first and the second drain electrodes **175***a* and **175***b*.

[0139] Referring to **FIGS. 34-35B**, a plurality of pixel electrodes **190** and a plurality of connecting members **85** are formed on the passivation layer **180**.

[0140] Referring to **FIGS. 36-37B**, a partition **32** and an auxiliary electrode **272** are formed by using a single photolithography step shown in **FIGS. 20A-22B**.

[0141] Finally, a plurality of organic light emitting members **30** preferably including multiple layers are formed in the openings by deposition or inkjet printing following a masking, and a common electrode **270** are subsequently formed as shown in **FIGS. 23-25**.

[0142] As described above, the formation of the partition **32** and the auxiliary electrode **272** with a single photolithography step simplifies the manufacturing process and thus reduces the manufacturing cost. In addition, this process facilitates to manufacture a large OLED.

[0143] Although preferred embodiments of the present invention have been described in detail hereinabove, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught which may appear to those skilled in the present art will still fall within the spirit and scope of the present invention, as defined in the appended claims.

What is claimed is:

1. An organic light emitting display comprising:

a first electrode formed on a substrate;

a partition having an opening exposing the first electrode at least in part;

an auxiliary electrode formed on the partition and having substantially the same planar shape as the partition;

an organic light emitting member formed on the first electrode and disposed substantially in the opening; and

a second electrode formed on the light emitting member and the auxiliary electrode.

2. The organic light emitting display of claim 1, further comprising:

a gate line transmitting gate signals;

a data line transmitting data signals;

a switching transistor connected to the gate line and the data line;

a signal transmission line transmitting driving signals; and a driving transistor connected to the signal transmission line and the first electrode and controlled by the data signals;

3. The organic light emitting display of claim 1, wherein the first electrode comprises reflective material.

4. The organic light emitting display of claim 1, wherein the second electrode comprises transparent material.

5. The organic light emitting display of claim 1, wherein the auxiliary electrode has a resistivity lower than the second electrode.

6. The organic light emitting display of claim 1, wherein the switching transistor and the driving transistor are connected to each other and the organic light emitting display further comprising a storage capacitor connected between the switching transistor and the signal transmission line.

7. An organic light emitting display comprising:

first and second semiconductor members including first and second intrinsic portions, respectively, and including amorphous silicon or polysilicon;

a plurality of gate conductors that include a gate line including a first gate electrode overlapping the first intrinsic portion and a second gate electrode overlapping the second intrinsic portion;

a gate insulating layer disposed between the first and the second semiconductor members and the gate conductors;

a plurality of data conductors that includes a data line including a first source electrode connected to the first semiconductor member, a first drain electrode opposing the first source electrode with respect to the first intrinsic portion and connected to the first semiconductor member, a voltage transmission line including a second source electrode connected to the second semiconductor member, and a second drain electrode opposing the second source electrode with respect to the second intrinsic portion and connected to the second semiconductor member;

a pixel electrode connected to the second drain electrode;

a partition having an opening exposing the pixel electrode at least in part;

an auxiliary electrode formed on the partition and having substantially the same planar shape as the partition;

an organic light emitting member formed on the pixel electrode and disposed substantially in the opening; and

a common electrode formed on the light emitting member and the auxiliary electrode.

8. The organic light emitting display of claim 7, wherein the pixel electrode comprises reflective material.

9. The organic light emitting display of claim 7, wherein the common electrode comprises transparent material.

10. The organic light emitting display of claim 7, wherein the auxiliary electrode has a resistivity lower than the common electrode.

11. The organic light emitting display of claim 7, further comprising a connecting member connecting the first drain electrode and the second gate electrode.

12. A method of manufacturing an organic light emitting display, the method comprising:

forming a plurality of first display electrodes;

forming a partition having a plurality of openings exposing the first display electrodes at least in part;

forming an auxiliary electrode on the partition;

forming a plurality of organic light emitting members in the openings; and

forming a second display electrode on the light emitting member and the auxiliary electrode,

wherein the formation of the partition and the formation of the auxiliary electrode are performed by using a single lithography.

13. The method of claim 12, wherein the formation of the partition and the formation of the auxiliary electrode comprise:

sequentially depositing an insulating layer and a conductively layer;

forming a first photoresist on the conductive layer;

sequentially etching the conductive layer and the insulating layer using the first photoresist as an etch mask to form a conductor and the partition;

ashing the first photoresist to form a second photoresist; and

etching the conductor to form the auxiliary electrode using the second photoresist as an etch mask.

14. The method of claim 1, wherein the first display electrodes comprise reflective material.

15. The method of claim 1, wherein the second display electrode comprises transparent material.

16. A method of manufacturing an organic light emitting display, the method comprising:

forming first and second semiconductor members including amorphous silicon or polysilicon;

forming a gate line including a first gate electrode and a second gate electrode;

forming a gate insulating layer between the first and the second semiconductor members and the gate line and the second gate electrode;

forming a data line including a first source electrode, a voltage transmission line, and first and second drain electrodes;

forming a passivation layer on the data line, the voltage transmission line, and the first and the second drain electrodes;

forming a pixel electrode on the passivation layer, the pixel electrode connected to the second drain electrode;

forming a partition having an opening exposing the pixel electrode at least in part;

forming an auxiliary electrode on the partition;

forming an organic light emitting member in the opening; and

forming a common electrode on the light emitting member and the auxiliary electrode.

17. The method of claim 16, wherein the formation of the partition and the formation of the auxiliary electrode comprise:

sequentially depositing an insulating layer and a conductively layer;

forming a first photoresist on the conductive layer;

sequentially etching the conductive layer and the insulating layer using the first photoresist as an etch mask to form a conductor and the partition;

ashing the first photoresist to form a second photoresist; and

etching the conductor to form the auxiliary electrode using the second photoresist as an etch mask.

18. The method of claim 16, wherein the pixel electrode comprises reflective material.

19. The method of claim 16, wherein the common electrode comprises transparent material.

20. The method of claim 16, wherein the auxiliary electrode has a resistivity lower than the common electrode.

* * * * *

专利名称(译)	有机发光显示器及其制造方法		
公开(公告)号	US20050127828A1	公开(公告)日	2005-06-16
申请号	US10/997996	申请日	2004-11-29
[标]申请(专利权)人(译)	钟金KOO CHOI JOON HOO CHOI BEOM RAK		
申请(专利权)人(译)	钟金辜 崔俊HOO 崔BEOM-RAK		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	CHUNG JIN KOO CHOI JOON HOO CHOI BEOM RAK		
发明人	CHUNG, JIN-KOO CHOI, JOON-HOO CHOI, BEOM-RAK		
IPC分类号	H01L51/50 G02F1/136 G09F9/30 G09G3/30 H01L27/32 H01L51/52 H01L51/56 H05B33/00 H05B33/08 H05B33/10 H05B33/12 H05B33/14 H05B33/26		
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外部链接	Espacenet USPTO		

摘要(译)

提供一种有机发光显示器，包括：形成在基板上的第一电极;具有开口的隔板，所述开口至少部分地暴露第一电极;辅助电极形成在隔板上并具有与隔板基本相同的平面形状;有机发光构件，形成在第一电极上并基本上设置在开口中;和形成在发光元件和辅助电极上的第二电极。